Ron Wade, John Hsu, Joe Tajnai, and Jagdeep Bal

1. Introduction

Historically, the preferred instrument for measuring the reference clock jitter of PCI Express® (PCIe®)[1] systems has been the digital storage oscilloscope (DSO). Unfortunately, as the data rates in successive PCIe generations increase and as reference clock maximum jitter specifications become lower, the DSO's intrinsic jitter is becoming a problem. The proposed jitter budget for the reference clock in a PCIe Gen5 system is 150fs max. This document will show that the intrinsic jitter of a scope takes almost this entire jitter budget. Secondly, this document will demonstrate that a phase noise analyzer (PNA) has a very low noise floor that is more than sufficient to measure reference jitter in PCIe Gen5 systems and beyond. And lastly, this document will compare PNA measurements and scope based measurements that seek to remove DSO intrinsic noise on the IDT9FGV1006.

In conclusion, this document will show that changes to the existing PCIe Gen3/4 filters are not required when using improved measurement techniques and low noise parts like the IDT9FGV1006.

Note: All PCIe rms jitter numbers are reported under the filter settings that result in the highest rms jitter. For more information, see Appendix C. Worst Case PCIe Filter Settings.

2. Digital Storage Oscilloscope (DSO) Intrinsic Jitter

Figure 1 shows the TIE rms jitter measured for a Wenzel source input. The rms jitter of a Wenzel source is specified at 36fs, all band (integrated over the entire range of possible modulation frequencies). The scope, due to its high noise floor, measures rms time interval error (TIE) as 1.3635ps. This 1.3635ps is due almost entirely to the intrinsic jitter or noise floor of the oscilloscope. The equation in Figure 2 can be used to convert this value to an equivalent phase noise floor.

Figure 1. RMS Jitter of a Wenzel Measured on a Keysight DSO S404A

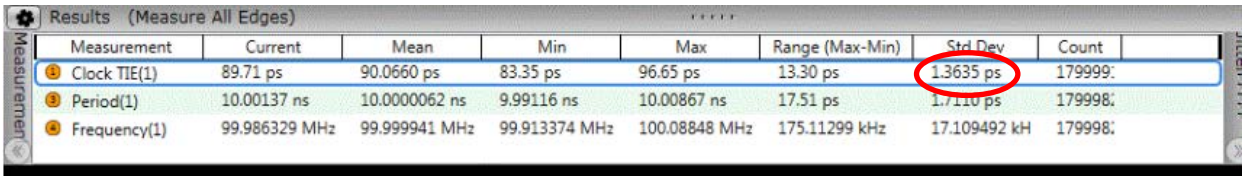


Figure 2. RMS TIE to Phase Noise Floor Conversion

$$Lt := 10 \log\left[\frac{(2 \cdot \pi \cdot rmsjitter)^2 \cdot fout}{2}\right] = -144.354 \quad \frac{dBc}{Hz} \qquad \text{(Equation 1)}$$

rmsjitter = TIE rms jitter, fout = Output frequency, Lt = Phase noise

[1] "PCI Express" and "PCIe" are registered trademarks of PCI-SIG.

Applying this noise floor to the PCIe filters results in the filtered rms jitter numbers shown in Figure 3. From this figure, one can see that the noise floor of the DSO filtered with the PCIe Gen4 common clock filter results in 186fs of integrated jitter. This is obviously too high a noise floor for PCIe Gen5 systems that will have a total jitter budget of 250fs. As a result, an alternative measurement technique is required for PCIe Gen5.

Figure 3. PCIe Filtered DSO Noise Floor

RMS Phase Jitters

Carrier: 100.000000 (MHz)

Sequence	Value(fs)	Limit(fs)	
PCIe2-CC-SSCG-LBW	9.93	3000.00	[PASS]
PCIe2-CC-SSCG-HBW	479.39	3100.00	[PASS]
PCIe2-IR-SSCG	593.84	2000.00	[PASS]
PCIe2-IR-SSCG	593.84	1000.00	[PASS]
PCIe3-CC-SSCG	186.28	1000.00	[PASS]
PCIe4-CC-SSCG	186.28	500.00	[PASS]
PCIe3/4-IR-SSCG	152.50	700.00	[PASS]

3. Phase Noise Analyzer (PNA) Measurement Floor

In contrast to the preceding discussion on DSO phase noise, the PNA measurement noise floor is quite low. Figure 4 shows the measurement noise floor of a PNA. Figure 5 shows that if the existing PCIe filters for Gen3/4 are used the measurement limit for common clocked (CC) systems would be 17.58fs.

Figure 4. PNA (R&S FSWP) Measurement Noise Floor (100MHz Input)

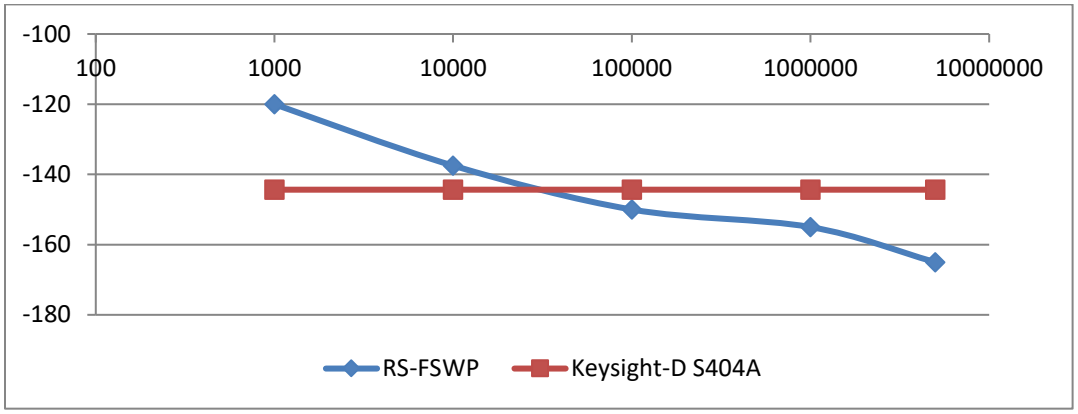


Figure 5. PCIe Filtered Noise Floor of the R&S FSWP

RMS Phase Jitters

Carrier: 100.000000 (MHz)

Sequence	Value(fs)	Limit(fs)	
PCIe2-CC-SSCG-LBW	3.31	3000.00	[PASS]
PCIe2-CC-SSCG-HBW	45.71	3100.00	[PASS]
PCIe2-IR-SSCG	60.92	2000.00	[PASS]
PCIe2-IR-SSCG	60.92	1000.00	[PASS]
PCIe3-CC-SSCG	17.58	1000.00	[PASS]
PCIe4-CC-SSCG	17.58	500.00	[PASS]
PCIe3/4-IR-SSCG	16.50	700.00	[PASS]

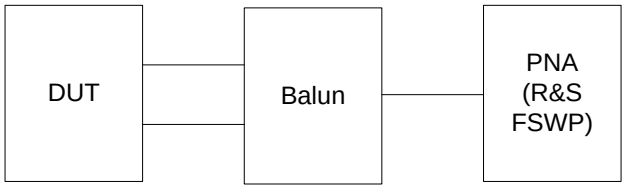
PCIe Gen5 rms jitter measurements with a PNA are straightforward due to the instrument's low noise floor and the fact that the PNA's frequency domain output can be directly applied to the PCIe filters.

4. Measuring PCIe Gen5 RMS Jitter of the IDT9FGV1006

4.1 PNA Method

To measure the PCIe rms jitter of the IDT9FGV1006 using a PNA, the setup in Figure 6 was used in the lab. Figure 7 shows the procedure to derive PCIE rms jitter from the PNA measurement.

Figure 6. PNA Measurement Setup



The IDT9FGV1006 measurements were taken with spread off and on. The measurements are summarized in Figure 6 and Figure 8. The reported results are for the filter settings that produced the highest rms jitter value. Figure 8 shows the PCIe rms jitter of a non-spread 100MHz output from the IDT9FGV1006. The results with spread on are displayed in Figure 9. As demonstrated in the measurement results, the IDT9FGV1006 in common clock mode has ample margin to the 150fs PCIe Gen5 specification.

Figure 7. Deriving Phase Noise from a PNA Measurement

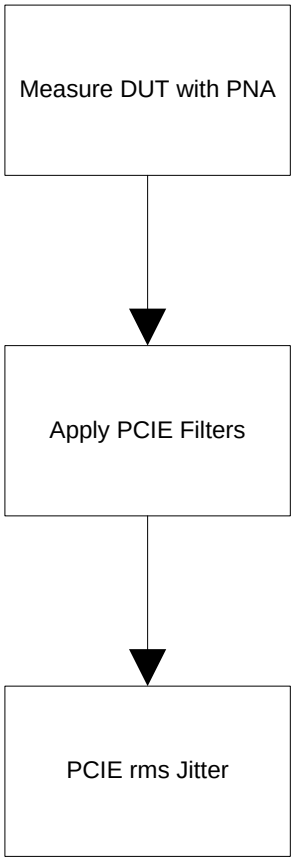


Figure 8. IDT9FGV1006 PCIe RMS Jitter with Spread Off, PNA Method

```
RMS Phase Jitters
------------------------------------------------------------
                               Carrier: 100.000000 (MHz)
------------------------------------------------------------
Sequence                      Value(fs)   Limit(fs)

PCIe2-CC-SSCG-LBW                 22.30     3000.00 [PASS]
PCIe2-CC-SSCG-HBW                194.27     3100.00 [PASS]
PCIe2-IR-SSCG                    251.64     2000.00 [PASS]
PCIe2-IR-SSCG                    251.64     1000.00 [PASS]
PCIe3-CC-SSCG                     86.52     1000.00 [PASS]
PCIe4-CC-SSCG                     86.52      500.00 [PASS]
PCIe3/4-IR-SSCG                   69.38      700.00 [PASS]
```

Figure 9. IDT9FGV1006 PCIe RMS Jitter with Spread On, PNA Method

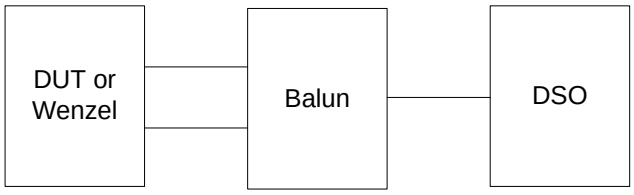
```
RMS Phase Jitters
-------------------------------------------------------
                                  Carrier: 100.000000 (MHz)
-------------------------------------------------------
Sequence                       Value(fs)   Limit(fs)

PCIe2-CC-SSCG-LBW                105.01     3000.00 [PASS]
PCIe2-CC-SSCG-HBW                294.87     3100.00 [PASS]
PCIe2-IR-SSCG                   1368.56     2000.00 [PASS]
PCIe2-IR-SSCG                   1368.56     1000.00 [FAIL]
PCIe3-CC-SSCG                    138.34     1000.00 [PASS]
PCIe4-CC-SSCG                    138.34      500.00 [PASS]
PCIe3/4-IR-SSCG                  515.41      700.00 [PASS]
```

4.2 DSO Based Measurements of the IDT9FGV1006

As has been discussed, the intrinsic noise in our DSO is too high to make PCIe Gen5 measurements directly. A technique must be developed that removes the intrinsic DSO noise. If the intrinsic noise of the DSO can be found then the noise of the DUT can be calculated. (Note: SUT = Signal under test; DUT = Device under test).

To determine the measurement noise floor of the DSO, the Keysight S404A, we used a Wenzel frequency source. The measurement setup is shown in Figure 10. Figure 11 shows the process used to cancel the scope intrinsic jitter.

Figure 10. Setup for DSO Based Measurements



The Wenzel has a very low noise floor. Its integrated PCIe Gen4 CC rms jitter is 13fs based upon its datasheet reported phase noise. The output noise measured by the scope with a Wenzel input is almost entirely comprised of the scope intrinsic noise. The mathematical relation to calculate the actual phase noise of the DUT with scope intrinsic noise removed is shown below. The detailed derivation of this equation is presented in Appendix B with supporting arguments in Appendix A.

$$Tj_m = \sqrt{(Tj_{SUT})^2 - \left(\frac{SR_{NS}}{SR_{SUT}} Tj_{NS}\right)^2}. \qquad \text{(Equation 2)}$$

$Tj_m = The\ rms\ jitter\ of\ the\ DUT\ with\ scope\ intrinsic\ jitter\ removed.$

$Tj_{SUT} = The\ total\ rms\ jitter\ measured\ by\ the\ DSO.$

$Tj_m = \sqrt{(Tj_{SUT})^2 - (Tj_{add})^2}$

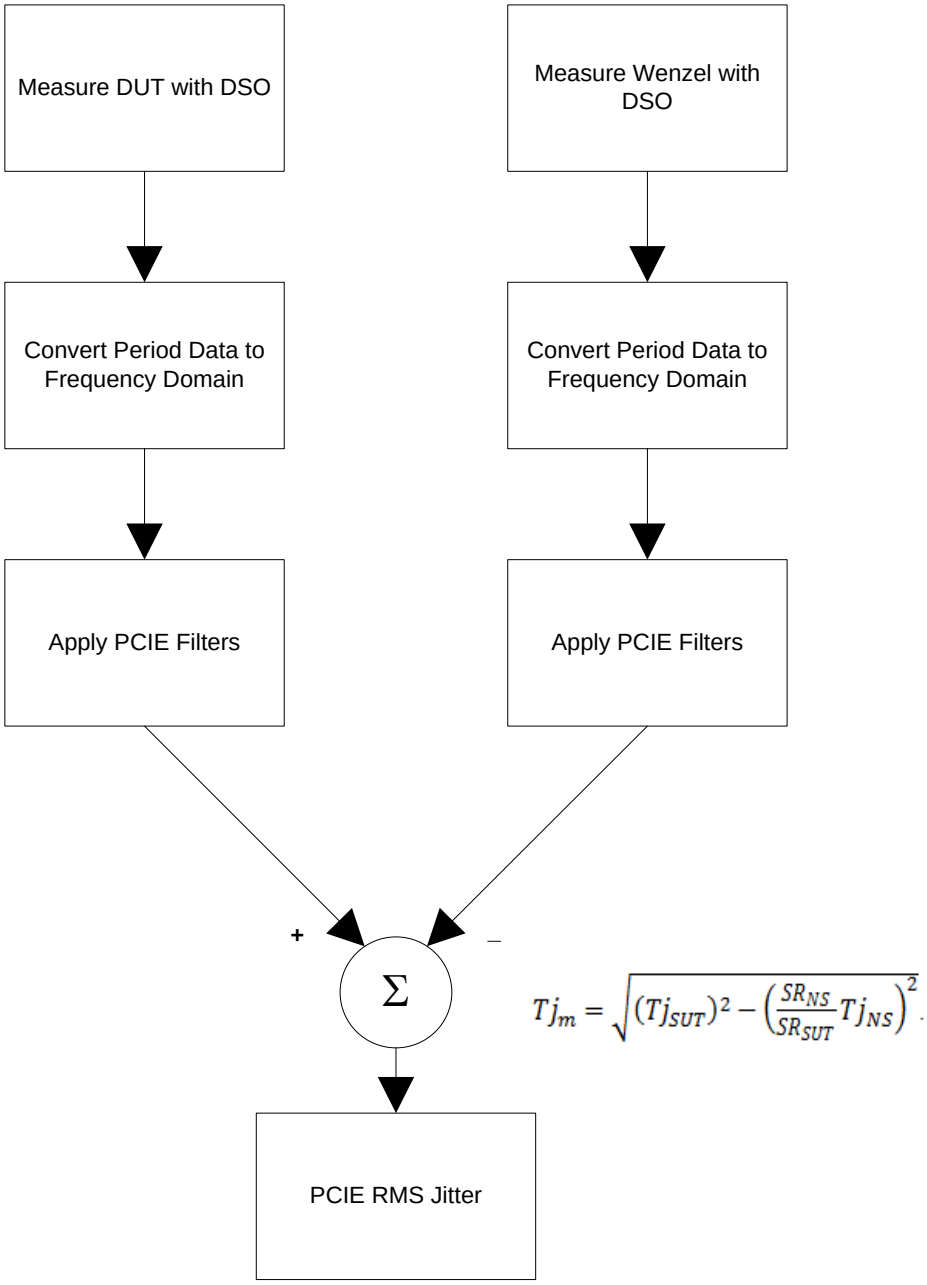
$Tj_{add} = The\ intrinsic\ jitter\ of\ the\ scope, Tj_{add} = \frac{SR_{NS}}{SR_{SUT}} Tj_{NS.}$

$Tj_{NS} = The\ rms\ jitter\ measured\ by\ the\ DSO\ with\ a\ Wenzel\ input, "Noiseless\ source."$

$SR_{NS} =$ The $slew\ rate\ of\ the\ Wenzel\ input.$

$SR_{SUT} =$ The $slew\ rate\ of\ the\ SUTapplied\ to\ the\ DSO.$

Figure 11. Removing Scope Noise from DUT Measurements



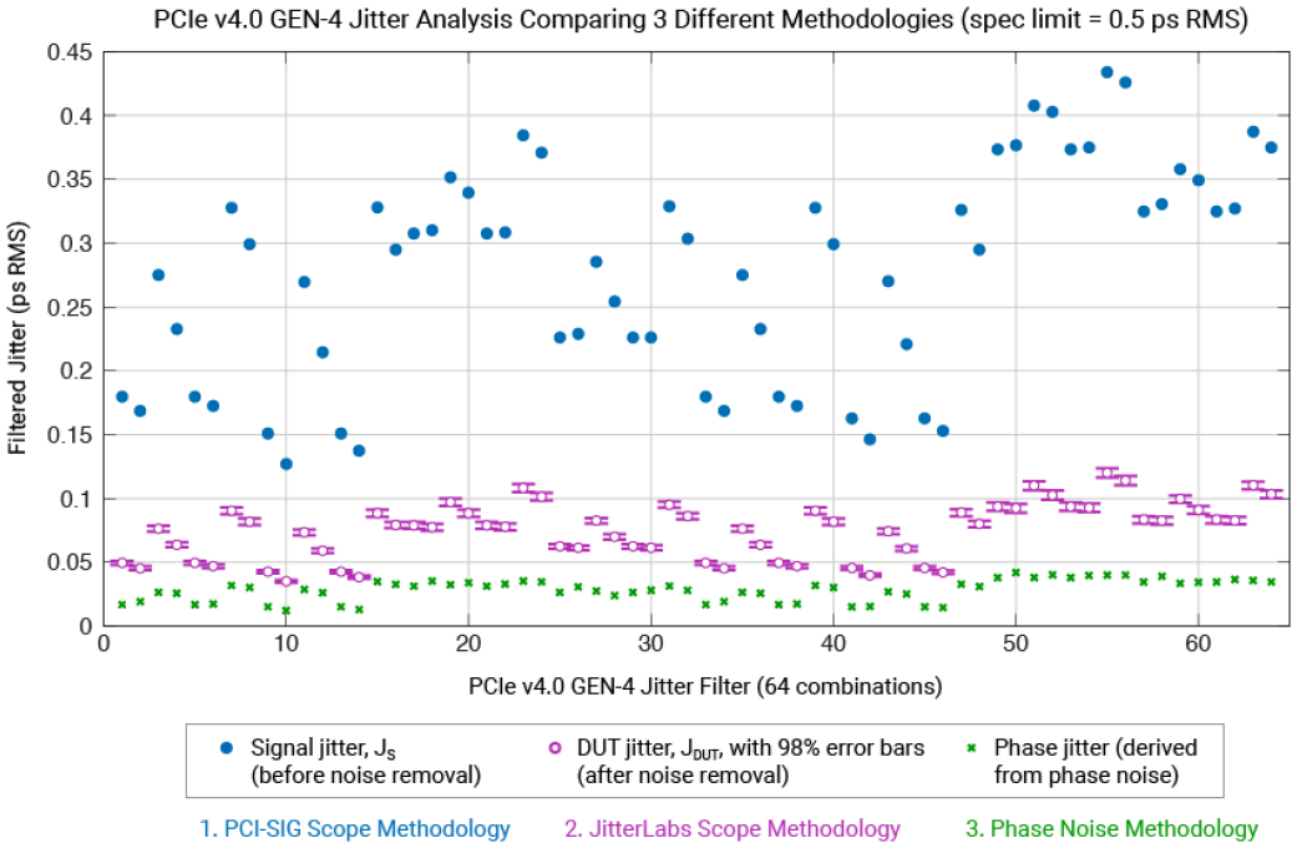
Using equation 2, the intrinsic noise of the DSO can be removed from scope based measurements and thus a DSO can be used to do PCIe Gen5 measurements. Table 1 summarizes our DSO based measurements on the IDT9FGV1006.

Table 1. Summary of DSO and PNA Based Measurements on the IDT9FGV1006 (Common Clock)

TJ_SUT (fSec)	SR_SUT (V/nSec)	TJ_NS (fSec)	SR_NS (v/nSec)	TJ_m (fSec)	Number of Periods	Spread	Method
253.05	0.979	81.72	2.68	118.27	200K	Off	DSO
279.31	0.979	81.69	2.68	167.35	1M	Off	DSO
279.21	0.979	81.72	2.68	167.07	2M	Off	DSO
NA	NA	NA	NA	86.52	NA	Off	PNA
264.17	0.979	76.67	2.68	160.42	2M	On	DSO
NA	NA	NA	NA	138.34	NA	On	PNA

To provide correlation for our method, we asked JitterLabs to use their DSO measurement method to do measurements on the same part in non-spread mode. Their results are shown in Figure 12. There is good correlation between the IDT and JitterLabs scope methodologies. In addition, the PNA methodologies are in agreement.

Figure 12. JitterLabs [Giust, 2017] DSO Measurement Results on the IDT9FGV1006 (Common Clock, Spread Off)



5. Conclusion

PCIe Gen4 filters can be used unchanged to meet Gen5 performance as long as care is taken to ensure a low noise floor in the measurement system and a low noise reference clock such as the IDT9FGV1006 is used. A phase noise measurement system such as the R&S FSWP has a low enough noise floor to measure PCIe Gen5 reference jitter. If a DSO is used, its intrinsic noise must be either low enough to be ignored or its intrinsic noise must be subtracted out from the measured result. In our experience, the PNA is the most straightforward way to achieve the desired PCIe filtered rms jitter result.

Appendix A. Mathematical Discussion of Phase Noise as Measured on the PNA and DSO

The notation of the following discussion is defined in Appendix A, of National Bureau of Standards technical note 632, and updated in the IEEE Std. 1139-1999. It is augmented with text book conventions; for example, the Fourier transform of h(t) is denoted as H(f).

A square wave with average frequency of v_0, and phase jitter of φ(t) has overall phase of

$$\Theta(t) = 2\pi v_0 t + \varphi(t)$$

in radians. Its average period is

$$\overline{\tau} = 1/v_0.$$

Phase jitter is normally measured in units of time. It is defined as

$$x(t) = \varphi(t)/2\pi v_0.$$

Therefore,

$$\Theta(t) = 2\pi v_0 t + \varphi(t) = 2\pi v_0 (t + x(t)).$$

Its phase can be approximately expressed as

$$\Theta(n\overline{\tau}) = 2\pi v_0 n\overline{\tau} + \varphi(n\overline{\tau}) = 2\pi v_0 (n\overline{\tau} + x(n\overline{\tau})).$$

That is, the phase of the square wave is measured at the zero cross over of each period. The rest of the discussion will use t for notation, where

$$t = n\overline{\tau}.$$

φ(t) and its Fourier transform, Φ(f) form a transform pair. Where f denotes Fourier frequency. Φ(f) cannot be readily measured. A signal's power spectral density (PSD) is measureable. PSD of a band limited signal is defined as

$$S_\Phi(f) = \Phi(f)\,\Phi^*(f)/BW$$

where $\Phi^*(f)$ is the complex conjugate of Φ(f) and BW is the measurement bandwidth. In the Fourier spectrum of the signal under test, $S_\Phi(f)$ is the two-sided noise spectrum about the carrier.

Phase Noise Analyzers demodulate and measure the single-sided phase noise spectrum, L(f), of the signals under test. Where

$$L(f) \equiv S_\Phi(f)/2$$

And they display

$$PN = 10\log_{10}(L(f))$$

in dBc/Hz. For a phase noise spectrum multiplied by a transfer function H(f), such as PCIe phase noise, PN can be calculated from the display with

$$PN = 10\log_{10}(L(f)) + 20\log(|H(f)|)$$

RMS jitter can be calculated from the equation

$$Tj = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN/10} df}$$

Alternatively, DSOs can be used to either measure phase jitter, Θ(n) , of the signal under test (SUT) by recording the time of zero cross over,

$\Theta(n) = (t_{0x}(n) - t_{0x}(n-1))/2\pi v_0$, [rad]

tox(n) = time of nth zero crossing

or p(n) of the SUT, the period jitter of the signal under test. Period jitter, which is basically phase jitter in seconds, p(n) can be calculated with

$p(n) = (t_{0x}(n) - t_{0x}(n-1)) - \overline{\tau}$, $n \geq 0 \cap n \epsilon I$

$x(j) = \sum_{n=n_0}^{j} p(n)$ is the accumulated phase jitter

The Fourier transform of the accumulated phase jitter can be calculated by

$X(f) = DFT(x(j))$. (1)

The maximum measureable modulation frequency of a SUT with frequency v_0 is its Nyquist rate,

$f_N = v_0/2$

This represents bimodal jitter in the time domain. For an FFT result with N bins, the bandwidth of each bin is

$\Delta f = f_N/N$

This is the measurement bandwidth of the phase noise spectrum. At this point, the phase noise spectrum of SUT can be calculated by the equation

$PN = 10log_{10}(L(f)) = 10log_{10}(S_\Phi(f)/2) = 20log_{10}(2\pi v_0 \sqrt{\frac{X(f)X^*(f)}{\Delta f}})$

Appendix B. Removing DSO Intrinsic Noise

DSOs have intrinsic voltage and other noises introduced by their component parts and architecture. DSO intrinsic noise is added to the phase or phase jitter measurements as additional phase noise. Calibration must be made to measure the noise, and subtract the noise from the overall measurement for a valid result. Even though voltage noise can be measured and recorded with a null input, other errors such as time base noise and quantization noise are hard to measure. The overall noise, as seen by the test setup, needs to be measured as phase or phase jitter, with a noiseless source (NS) at the input to the overall test setup. For PCIe measurement, a Wenzel signal source is quiet enough to be considered noiseless. There are other examples in the marketplace as well.

To calibrate with a noiseless source, obtain $X_{NS}(f)$ (Fourier transform of the phase jitter of a noiseless source) as in (1) and measure the signal slew rate seen by the test setup of both the noiseless source, SR_{NS}, and the signal under test, SR_{SUT}. The phase noise power spectrum measured by the noiseless source is

$$|X_{NS}(f)| = \sqrt{X_{NS}(f){X_{NS}}^{*}(f)}$$

The additive phase noise from the measurement setup is (see section 3.2 for variable definitions),

$$|X_e(f)| = \frac{SR_{NS}}{SR_{SUT}}\sqrt{X_{NS}(f){X_{NS}}^{*}(f)} = \frac{SR_{NS}}{SR_{SUT}}|X_{NS}(f)|.$$

The above corrects for the DSO intrinsic noise sensitivity to input slew rate. Phase noise filtered with a transfer function H(f), is given by $PN_f(f)$ where,

$$PN_f(f) = 10log_{10}\left[\left(2\pi v_0 \frac{|X(f)||H(f)|}{\sqrt{\Delta f}}\right)^2\right].$$

Phase noise of the SUT and the noiseless source (NS) can both be filtered as above.

$$PN_{SUT}(f) = 10log_{10}\left[\left(2\pi v_0 \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2\right]$$

$$PN_{add}(f) = 10log_{10}\left[\left(2\pi v_0 \frac{SR_{NS}}{SR_{SUT}} \frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2\right]$$

RMS jitter of the above can be calculated as,

$$Tj_{SUT} = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_{SUT}(f)/10} df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df}$$

$$Tj_{add} = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_{add}(f)/10} df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{SR_{NS}}{SR_{SUT}} \frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df}$$

$$= \frac{SR_{NS}}{SR_{SUT}}\frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df} = \frac{SR_{NS}}{SR_{SUT}} Tj_{NS}$$

The calibrated phase noise measurement, PN_m is then

$$PN_m(f) = 10log_{10}\left[(2\pi v_0 \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}})^2 - (2\pi v_0 \frac{SR_{NS}}{SR_{SUT}} \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}})^2\right].$$

RMS jitter from the measurement is then

$$Tj_m = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_m(f)/10} df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left[\left(2\pi v_0 \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 - \left(2\pi v_0 \frac{SR_{NS}}{SR_{SUT}} \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2\right] df}$$

$$= \sqrt{\left(\frac{1}{2\pi v_0}^2\right) 2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df - \left(\frac{1}{2\pi v_0}^2\right) 2\int_{f1}^{f2}\left(2\pi v_0 \frac{SR_{NS}}{SR_{SUT}} \frac{|X_{SUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df}$$

$$= \sqrt{(Tj_{SUT})^2 - (Tj_{add})^2}$$

$$= \sqrt{(Tj_{SUT})^2 - \left(\frac{SR_{NS}}{SR_{SUT}} Tj_{NS}\right)^2}$$

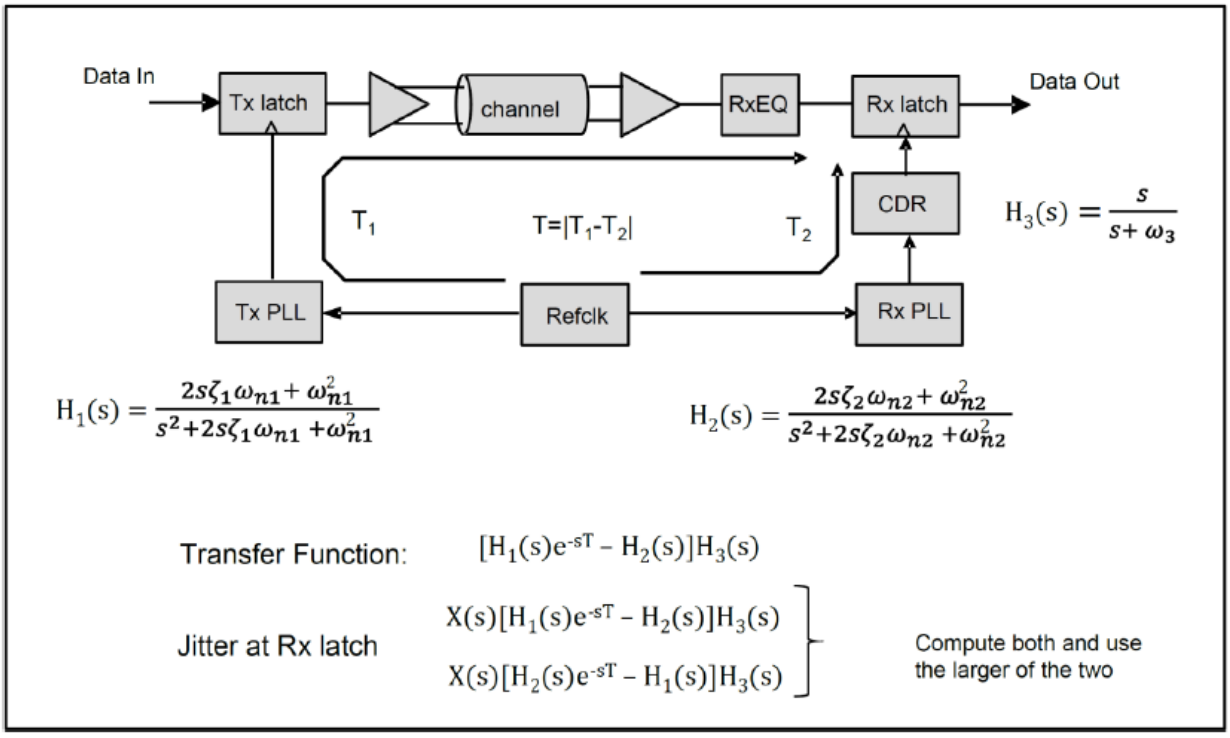
Appendix C. Worst Case PCIe Filter Settings

The worst case filter settings for spread on and spread off settings of the IDT9FGV1006 are shown below.

Table 2. Worst Case PCIe Filter Settings

Spread	H1 Peaking	H1 BW	H2 Peaking	H2 BW
OFF	0dB	5M	0dB	5M
ON	2dB	2MHz	1dB	5MHz

Figure 13. Calculating Worst Case PCIe Filter Settings



Note: The above diagram is from *PCI Express Base Specification, Revision 4.0, Version 1.0*.

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Revision History

Revision Date	Description of Change
October 17, 2019	Updated the proposed jitter budget for the reference clock in a PCIe Gen5 system from 250fs to 150fs.
January 9, 2018	Updated to include additional trademark information.
December 20, 2017	Initial release.

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