


# IDT PLL BGA CHIP CARRIER

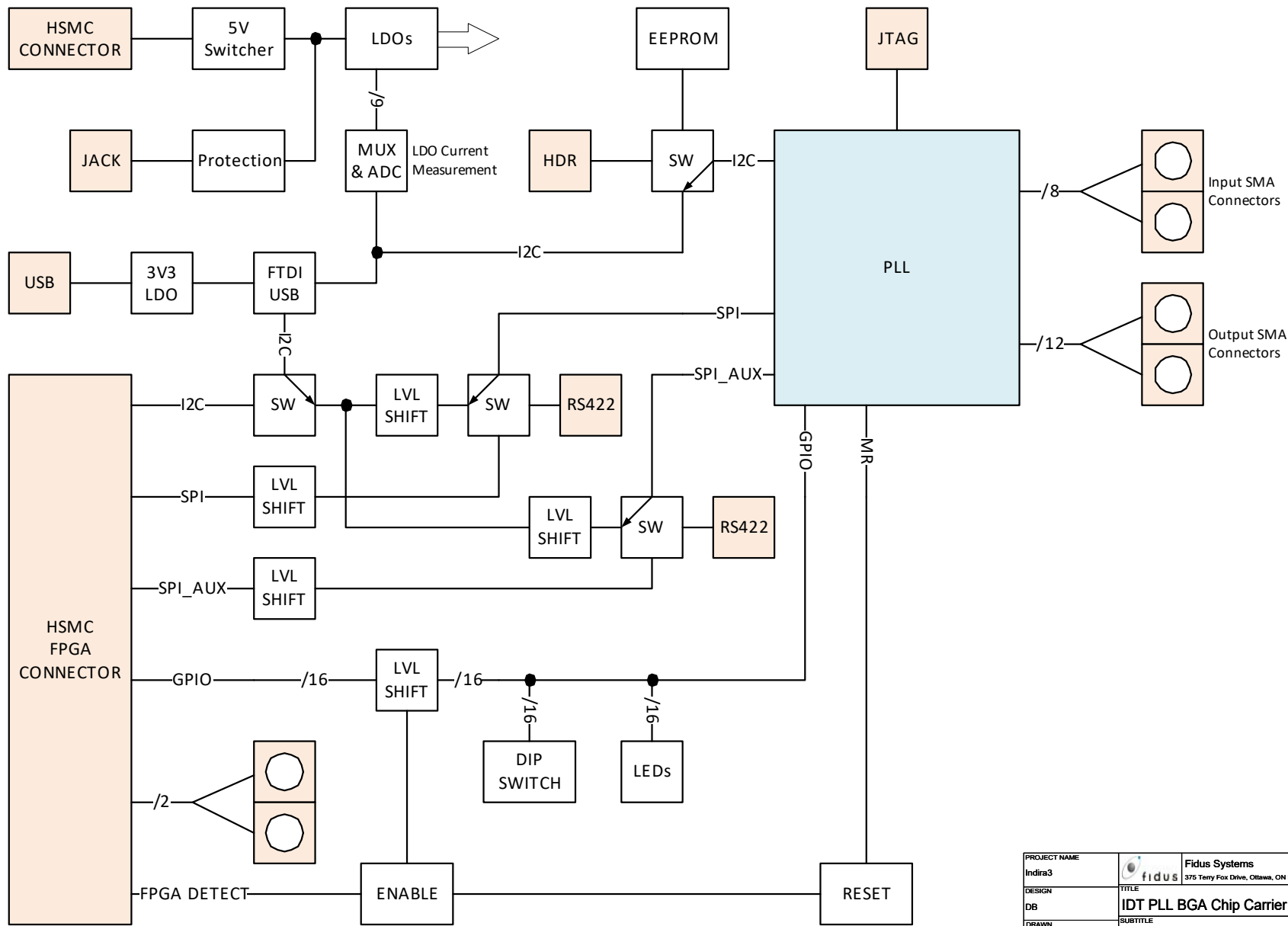
## TABLE OF CONTENTS

PAGE	DESCRIPTION
1	Table of Contents and Revision History
2	Block Diagram
3	Power Supplies 1
4	Power Supplies 2
5	Power Supplies 3
6	Current Measurement
7	FTDI USB Interface
8	Backplane Connector
9	PLL Core
10	GPIO DIP SW
11	PLL Output Clocks
12	PLL Power
13	PLL Input Clocks
14	GPIO LEDs
15	PLL SPI Select
16	PLL AUX SPI Select

## REVISION HISTORY

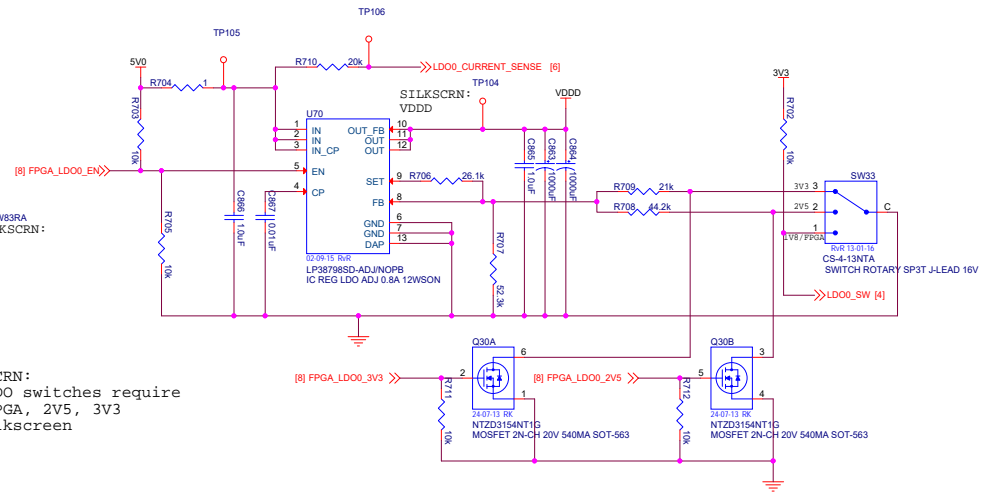
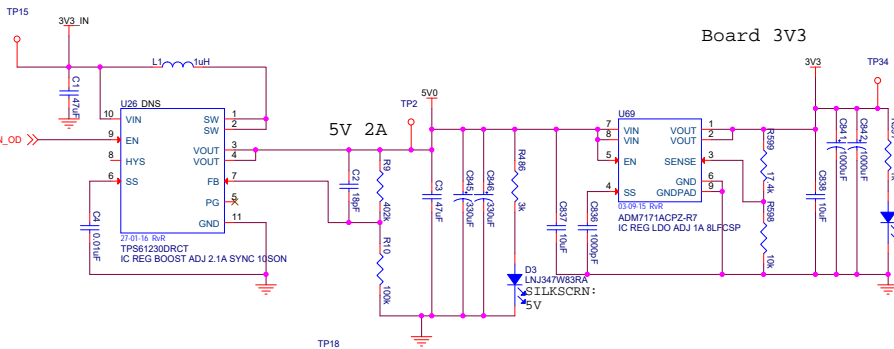
REVISION	DATE	CHANGE DETAILS
0.1	14 September 2016	First Release
0.2	16 September 2016	Updates to 5V0 input, EEPROM connections, and SPI selection pages.
0.3	19 September 2016	Added individual filters on VDDO lines. Removed J27 & J28. Added SMA on output of Y4.
0.4	19 September 2016	Added 0 Ohm resistors in series with inductors for U58 power supply filtering.
0.5	19 September 2016	Removed U79, U89, and FTDI_PLL_CS signal.
0.6	21 September 2016	C761 connected to GND.
0.7	22 September 2016	Added J83 and J84 for external I2C access.
0.8	11 October 2016	Removed J84. Updated block diagram.
0.9	11 October 2016	Updated title blocks. Update to block diagram. Corrected names of VDDO nets.
0.10	17 October 2016	Power supply changes. Changes to input and output clock terminations.
0.11	17 October 2016	Changed R910 to stuffed, 2.67k. Connected C795 to 3V3_IN.
1.0	27 October 2016	Release for build This version built November, 2016
1.1	7 March 2017	Changed SPI level shifters to TI TXB0104 parts Changed EEPROM to Microchip 24LC64 part
1.2	10 April 2017	BoM changes as per emails from Leon, 4 April 2017, and 10 April 2017.

PROJECT NAME	Indira3		 <b>Fidus Systems</b> <small>375 Terry Fox Drive, Ottawa, ON K2K 0J8</small>	
DESIGN	DB			
TITLE	<b>IDT PLL BGA Chip Carrier</b>			
DESIGN	DB			
DRAWN	DB			
SUBTITLE		Table of Contents and Revision History		
DRAWING NUMBER		SK-10280-01		
CHECK	RELEASE DATE		REVISION	
DB	27 October 2016		1.2	
SHEET			1 OF 16	

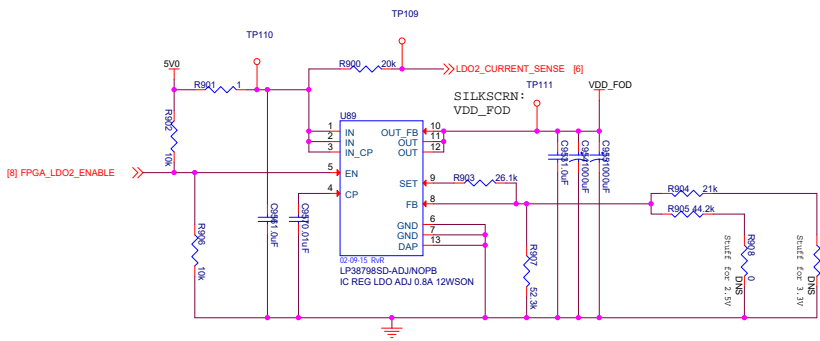
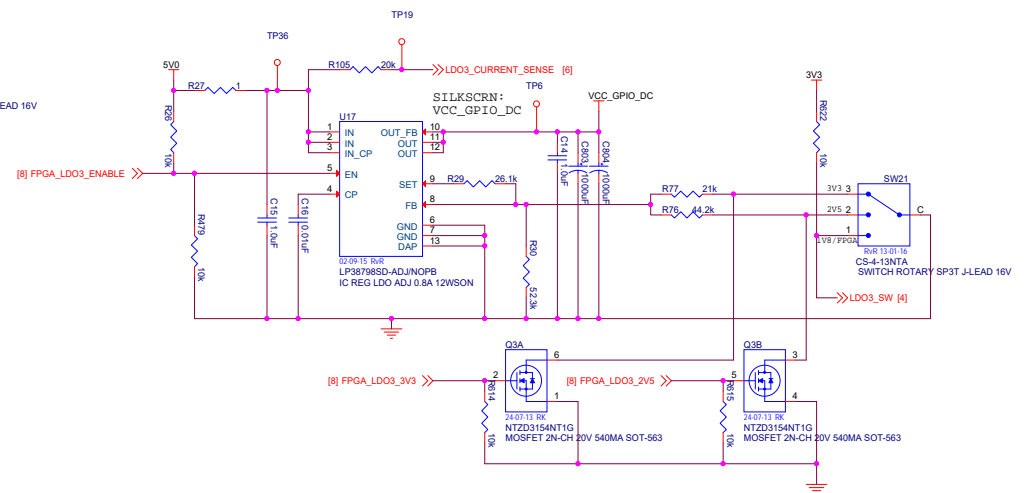
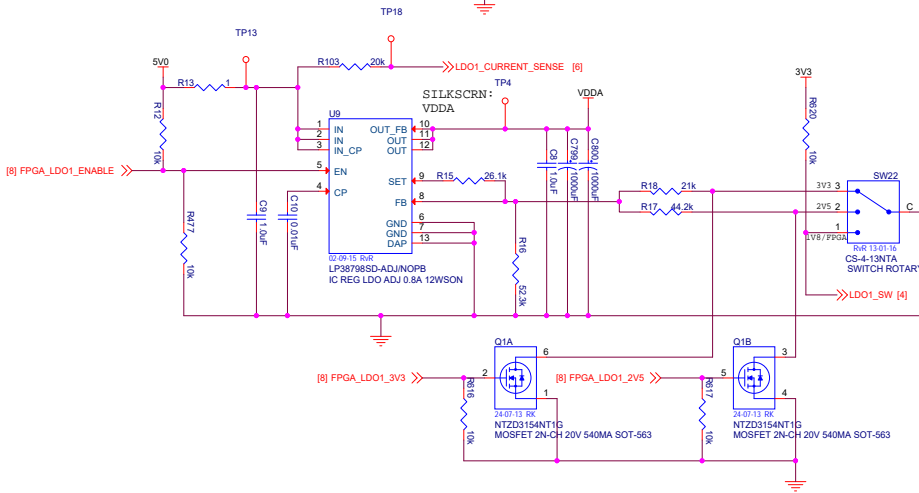


PROJECT NAME	Indira3		Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN	TITLE IDT PLL BGA Chip Carrier			
DB	SUBTITLE Block Diagram			
DRAWN	DRAWING NUMBER SK-10280-01			REVISION 1.2
CHECK	RELEASE DATE 27 October 2016			SHEET 2 OF 16
DB				

### Board 3V3



SILKSCRN:  
All LDO switches require  
1V8/FPGA, 2V5, 3V3  
in silkscreen

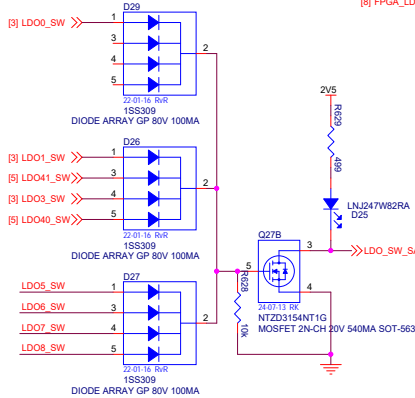
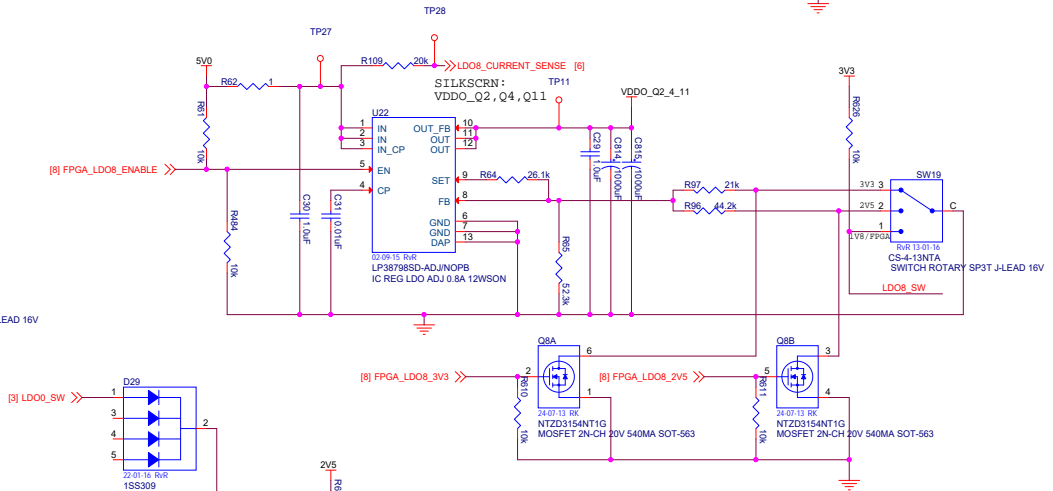
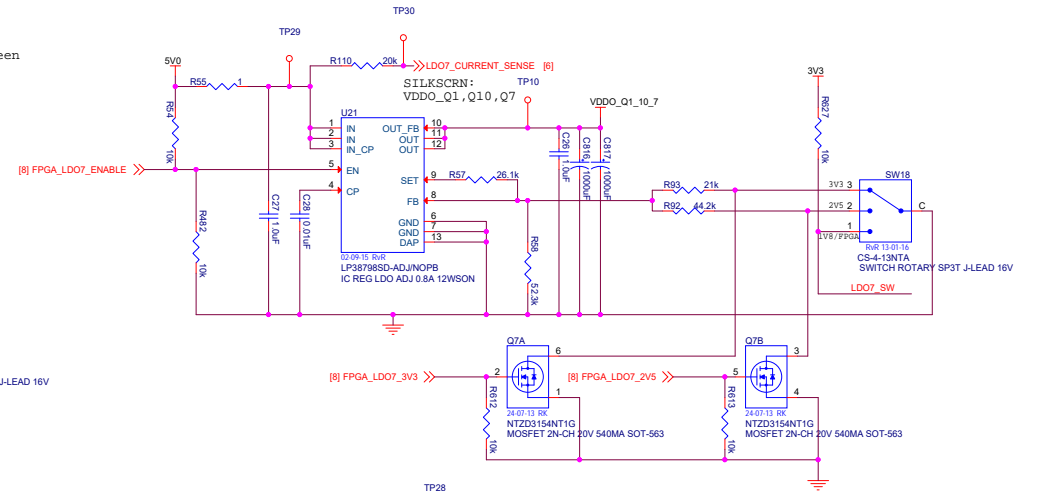
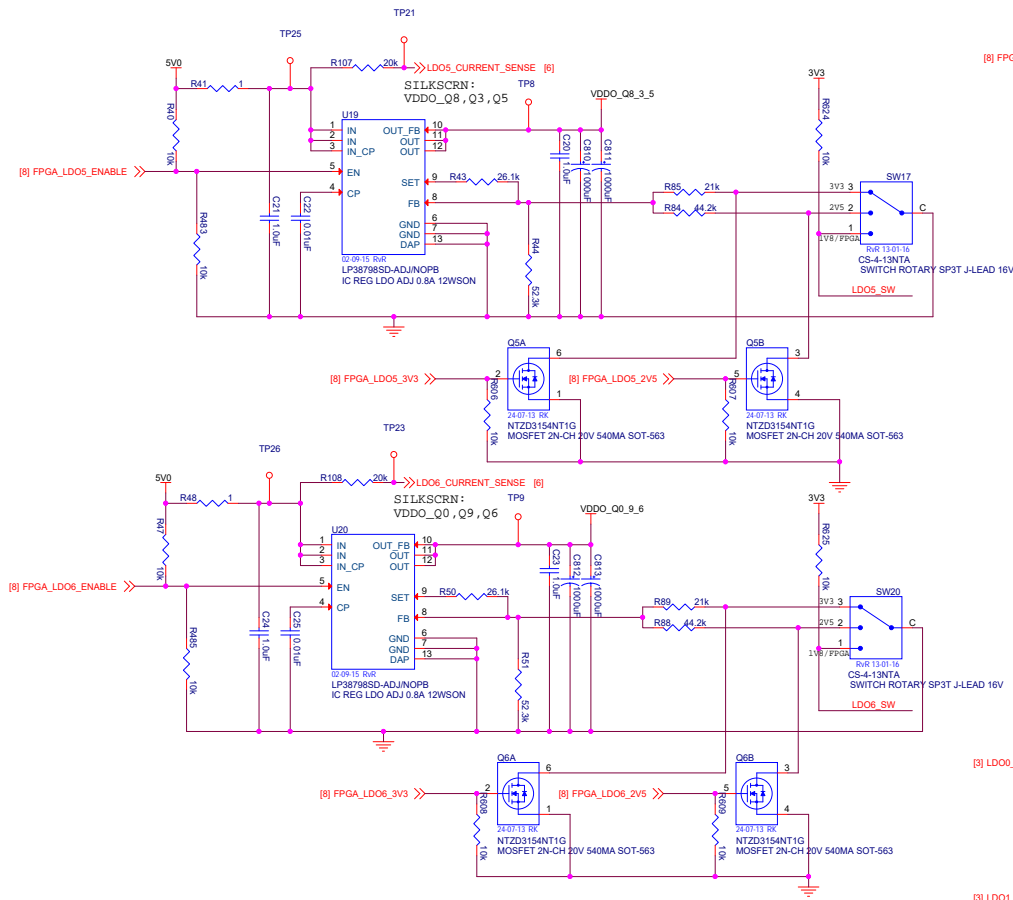


### LDO Switch Legend

- POS 3 = 3V3
- POS 2 = 2V5
- POS 1 = 1V8/FPGA control

PROJECT NAME	Indra3		
DESIGN	IDT PLL BGA Chip Carrier		
DRAWN	Power Supplies 1		
DB	DRAWING NUMBER		REVISION
CHECK	SK-10280-01		1.2
DB	RELEASE DATE	SHEET	3 OF 16
	27 October 2016		

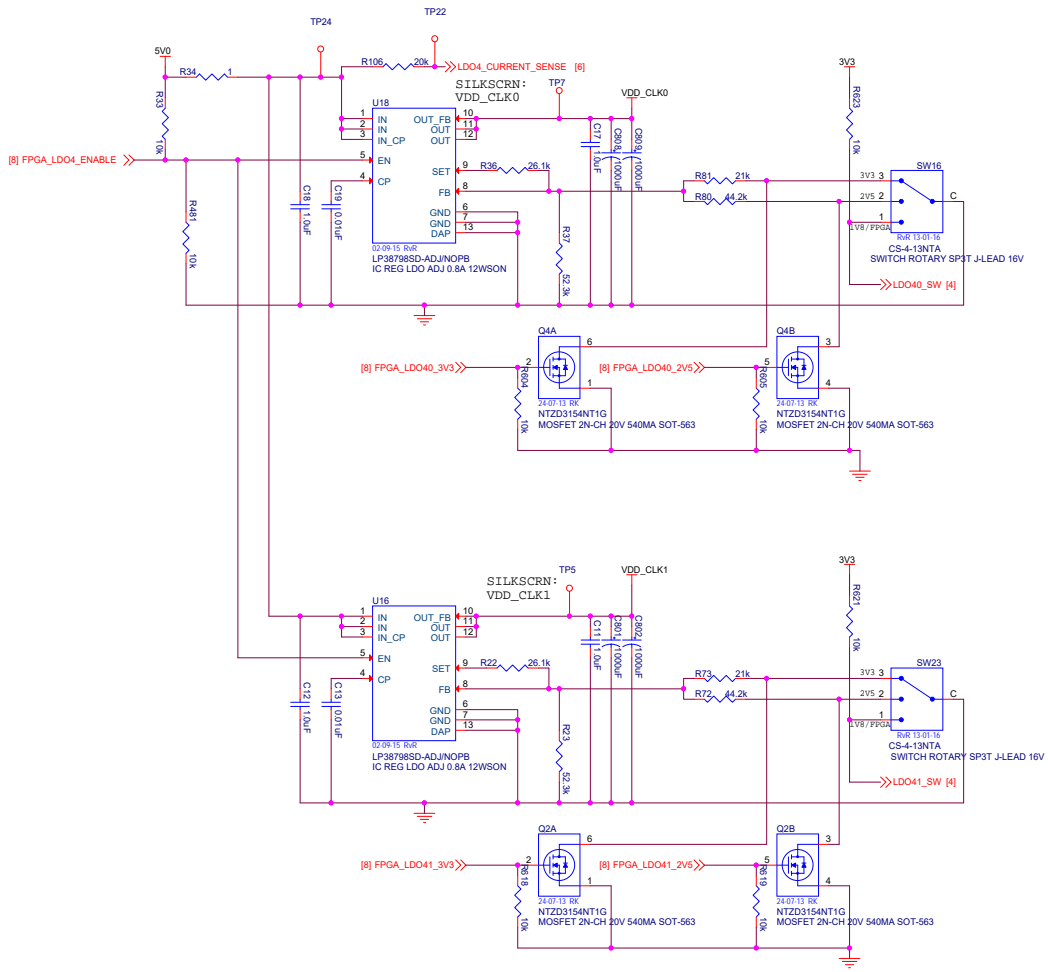
SILKSCRN:  
All LDO switches require 1V8/FPGA, 2V5, 3V3 silkscreen



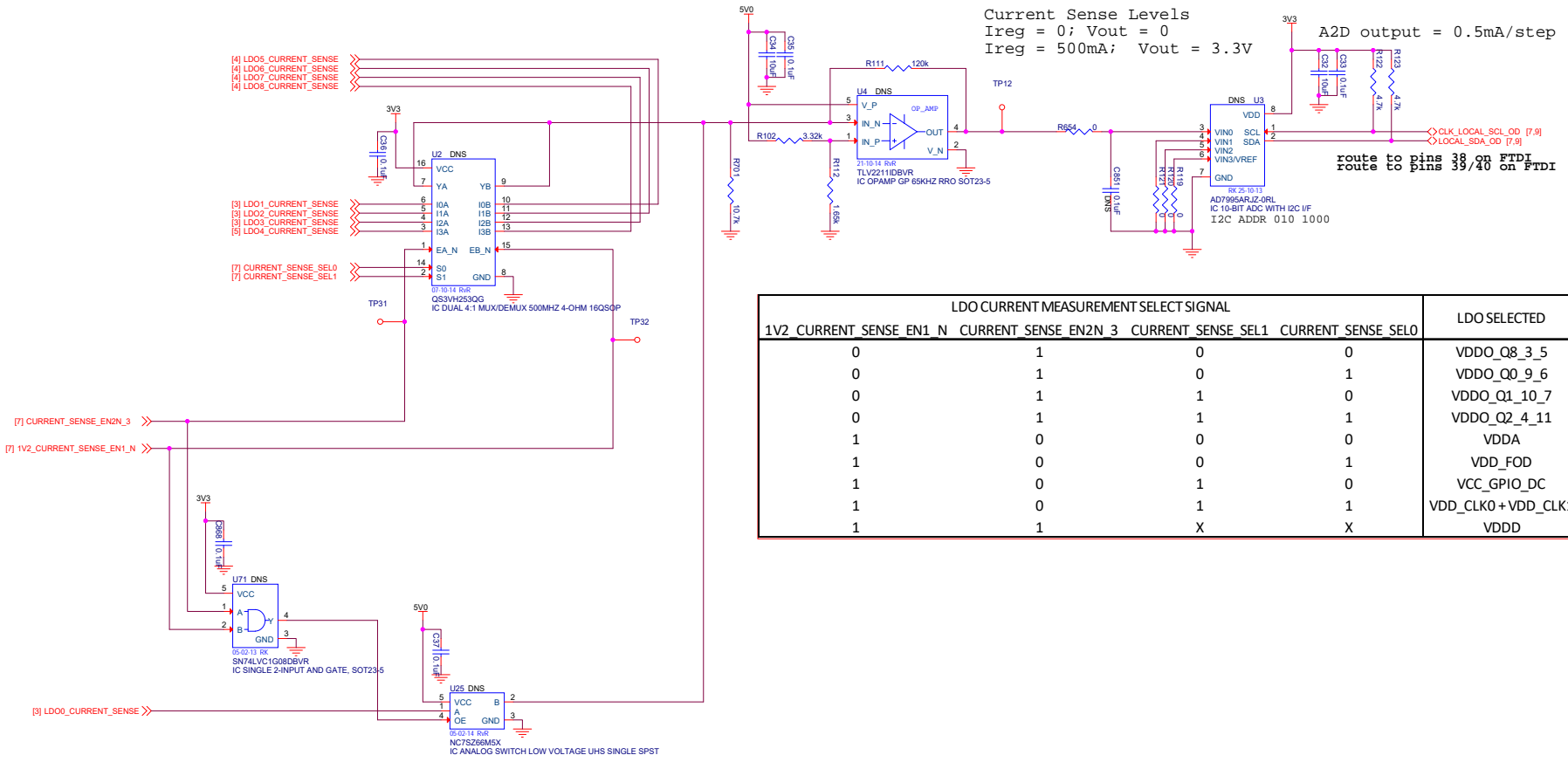
SILKSCRN :  
FPGA\_CTRL\_DIS

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DB	DRAWING NUMBER SK-10280-01	
CHECK	RELEASE DATE	REVISION
DB	27 October 2016	1.2
SHEET		4 OF 16

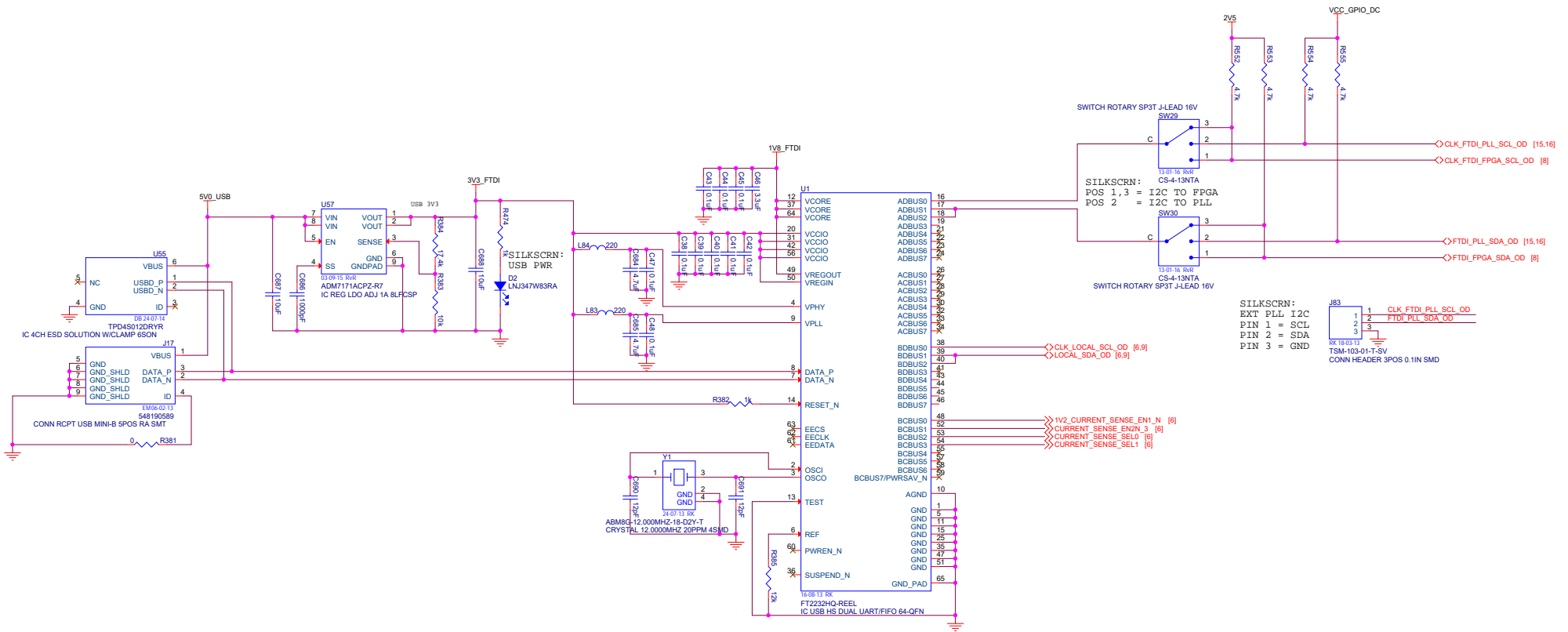
SILKSCRN:  
All LDO switches require 1V8/FPGA, 2V5, 3V3 silkscreen



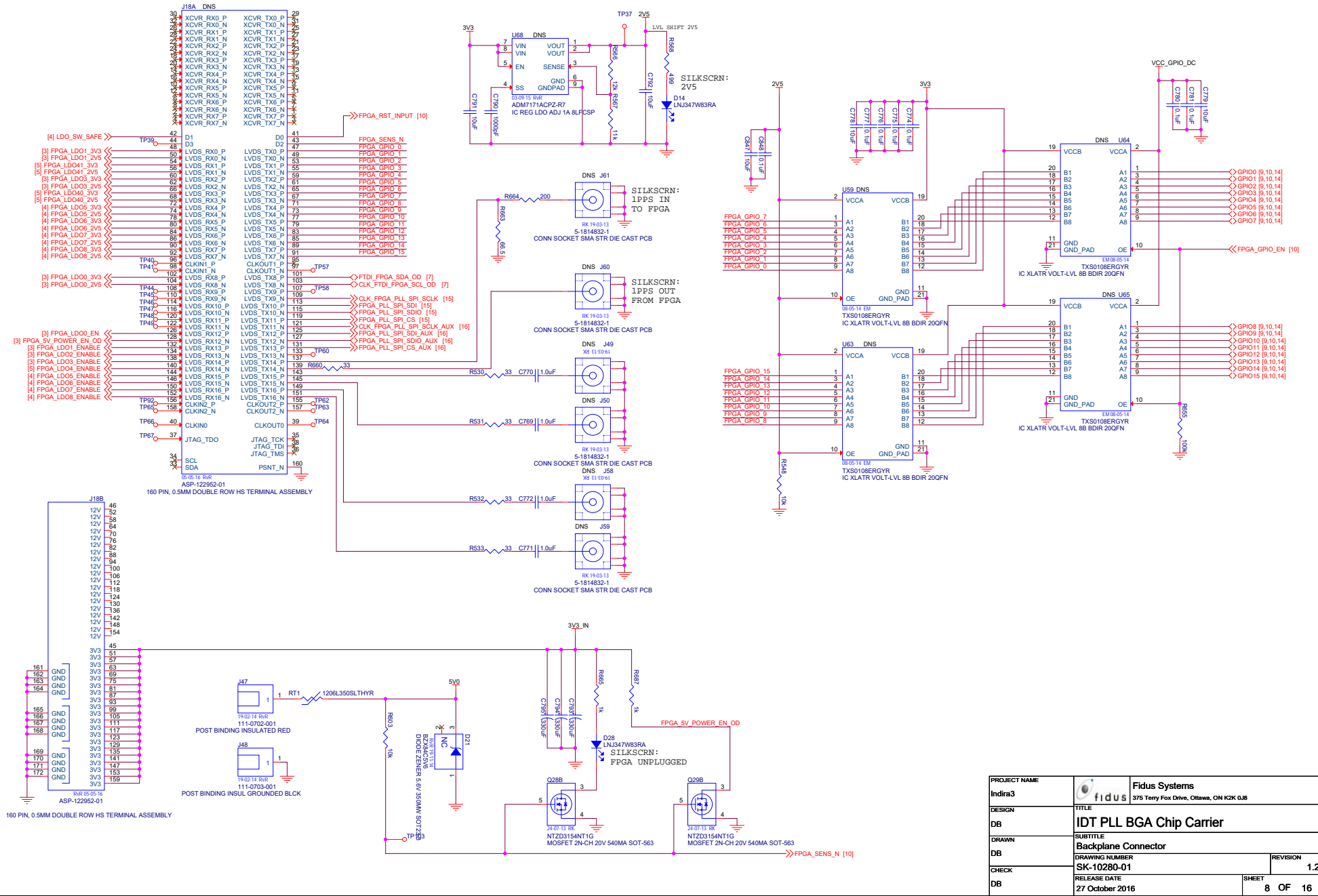
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RK	Power Supplies 3	
CHECK	DRAWING NUMBER	REVISION
DB	SK-10280-01	1.2
	RELEASE DATE	SHEET
	27 October 2016	5 OF 16



PROJECT NAME	Indira3		Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN	IDT PLL BGA Chip Carrier			
DRAWN	SUBTITLE Current Measurement			
CHECK	DRAWING NUMBER SK-10280-01		REVISION 1.2	
DB	RELEASE DATE 27 October 2016		SHEET 6 OF 16	

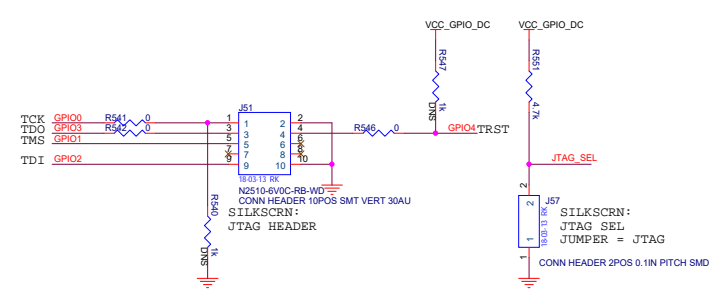
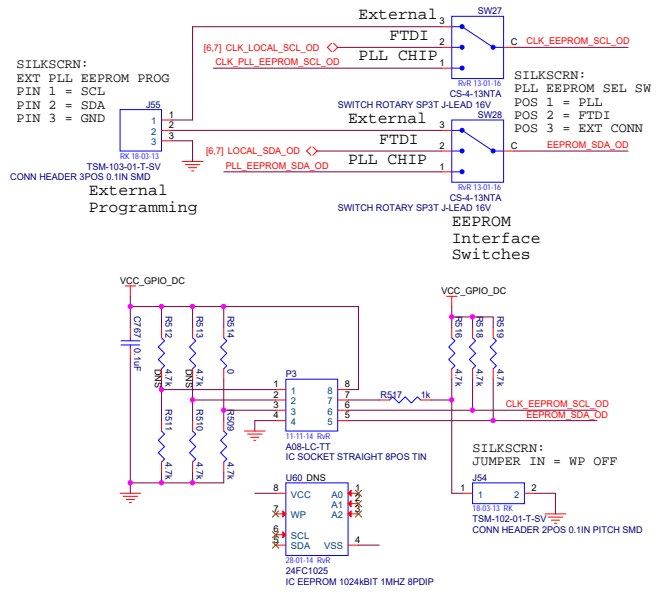
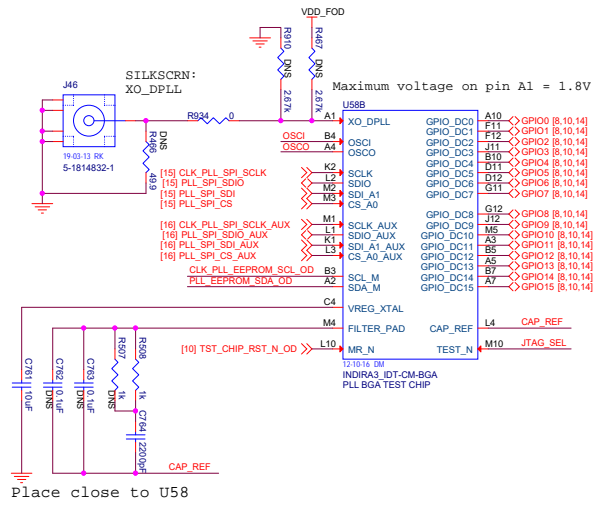
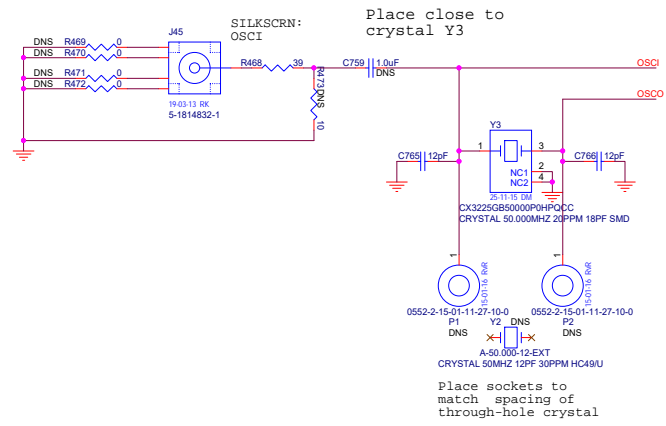


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DRAWN	SUBTITLE			
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DB	DRAWING NUMBER			1.2
CHECK	SK-10280-01			RELEASE DATE
DB	27 October 2016			SHEET 7 OF 16

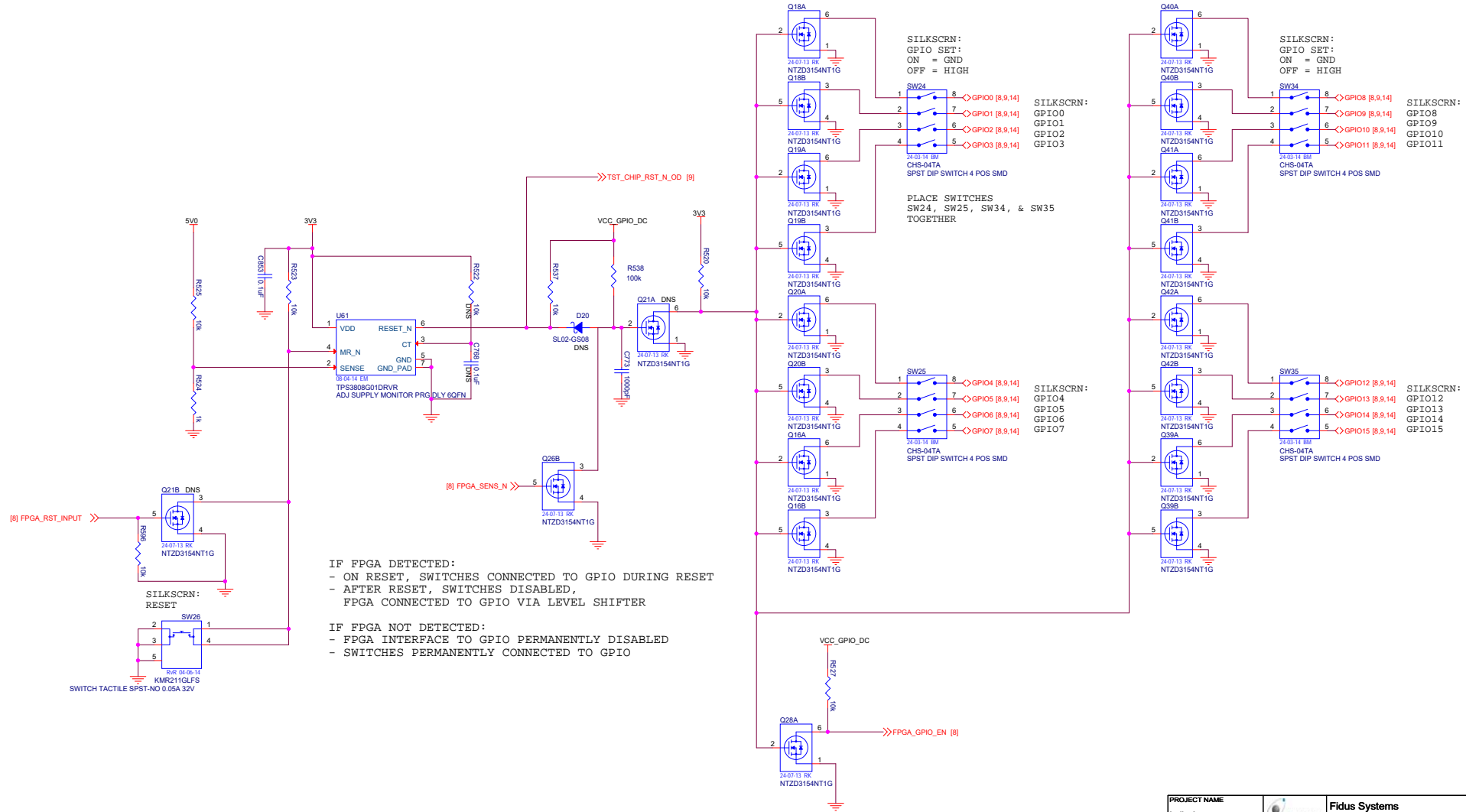


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DRAWN	SUBTITLE Backplane Connector	
DB	DRAWING NUMBER SK-10280-01	
CHECK	RELEASE DATE	REVISION
DB	27 October 2016	1.2
SHEET		8 OF 16



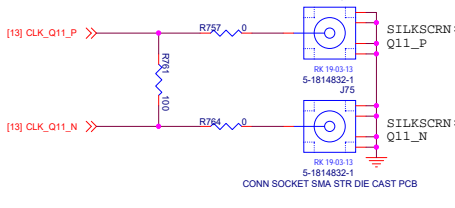
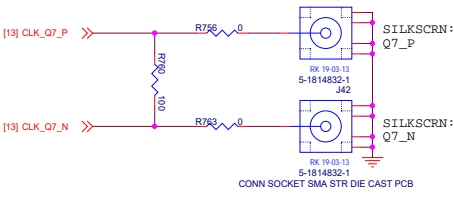
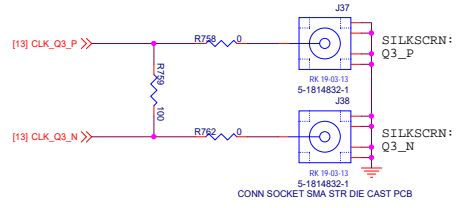
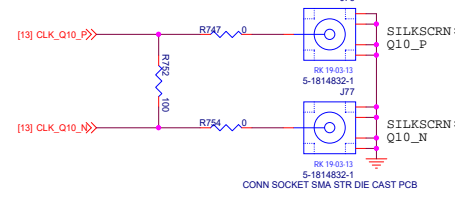
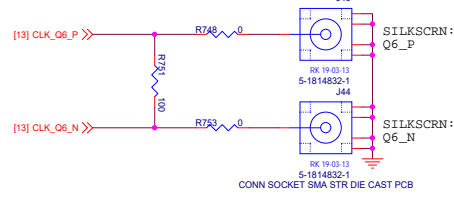
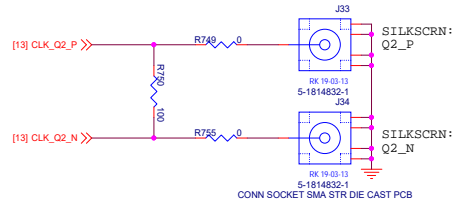
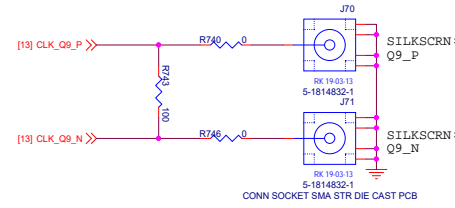
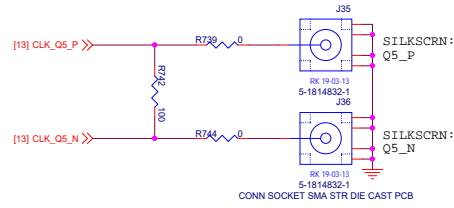
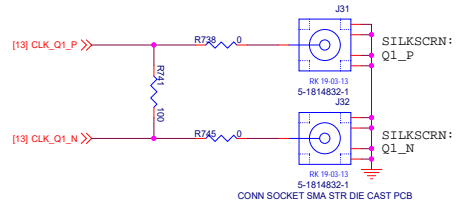
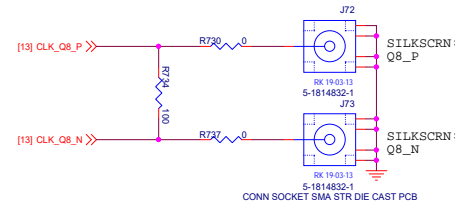
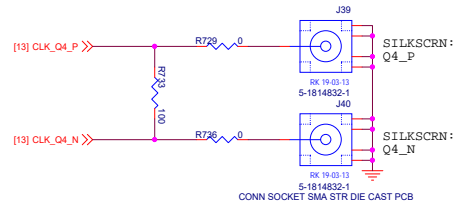
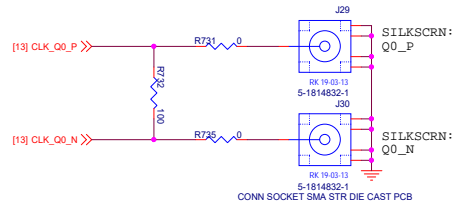


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DB	9 OF 16	REVISION
	1.2	

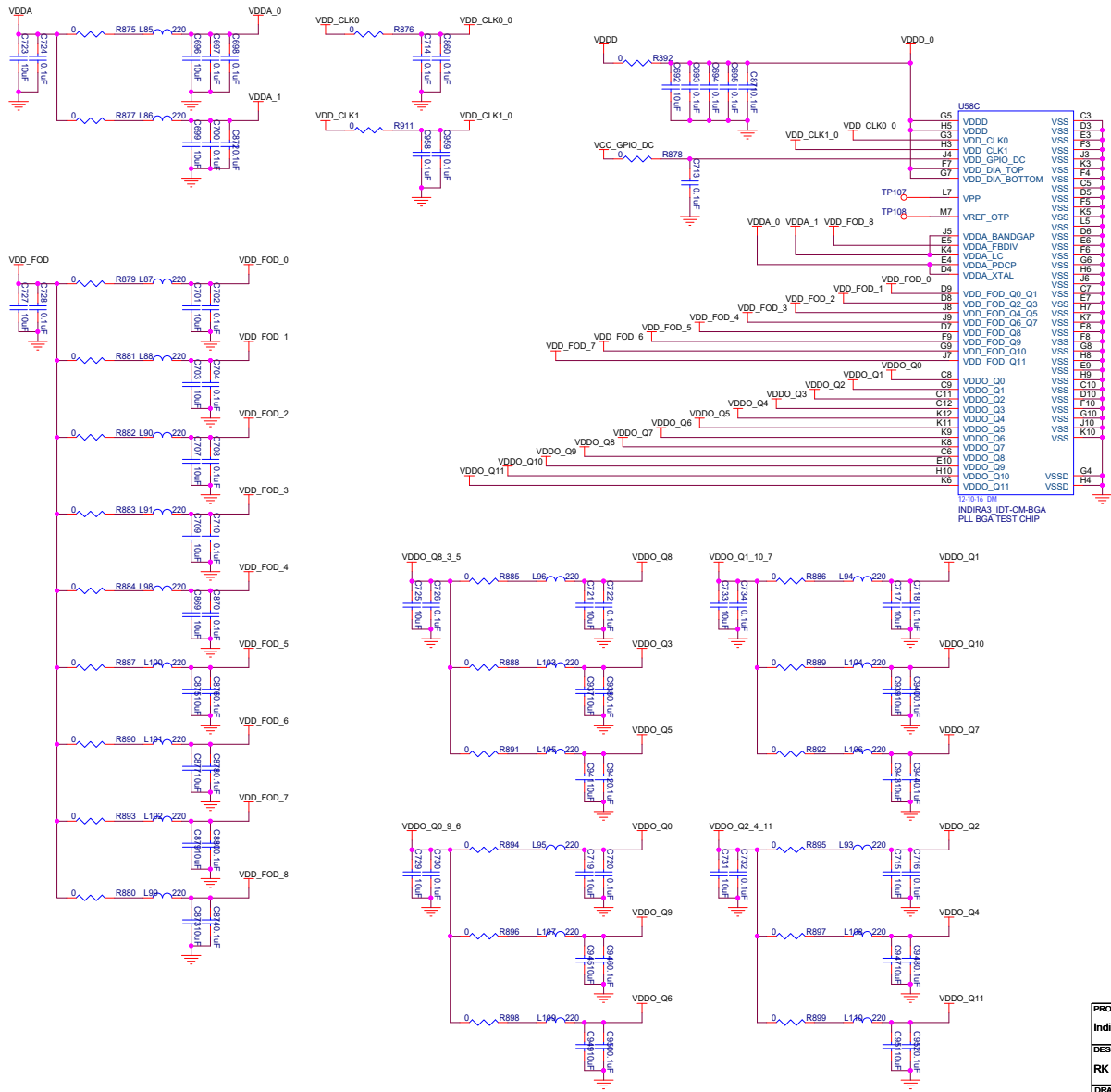



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DRAWN	SUBTITLE	
DB	GPIO DIP SW	
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DB	SK-10280-01	1.2
	RELEASE DATE	SHEET
	27 October 2016	10 OF 16

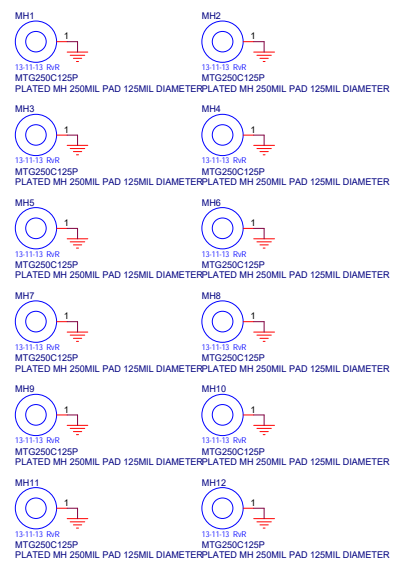
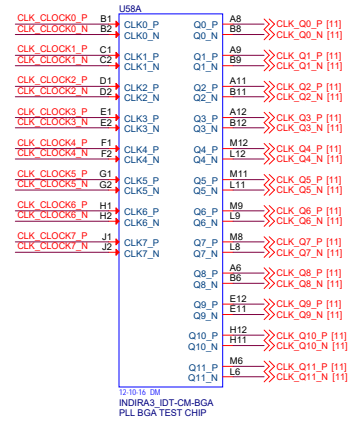
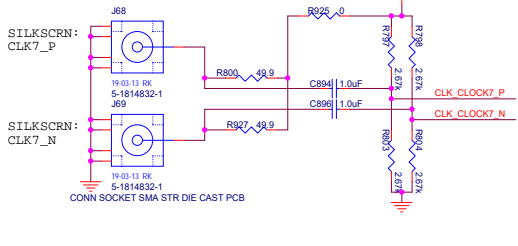
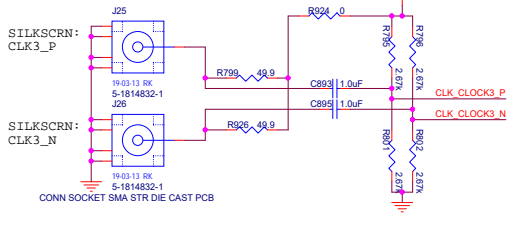
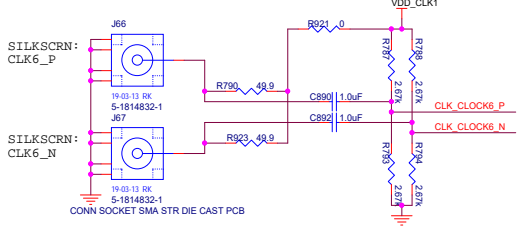
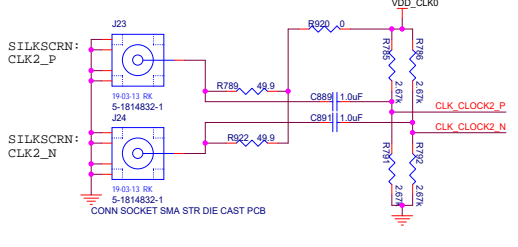
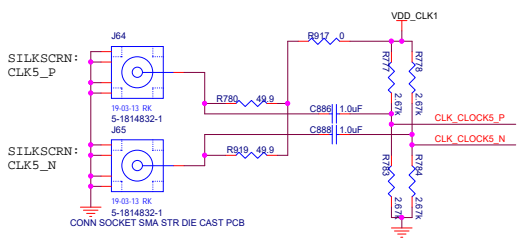
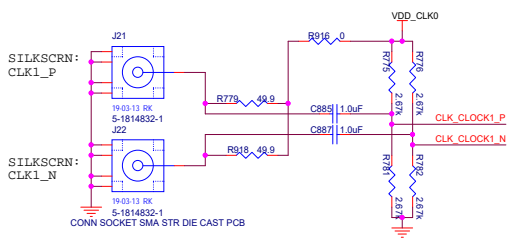
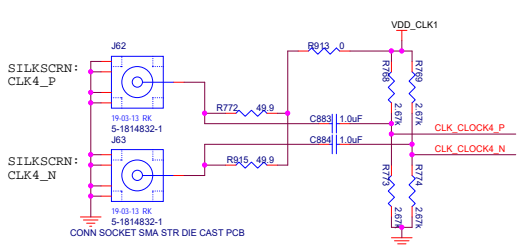
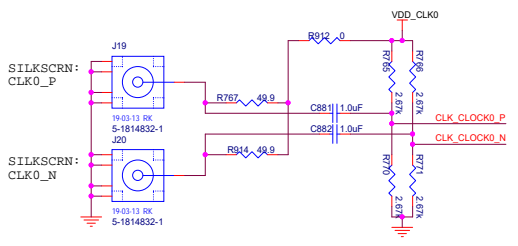
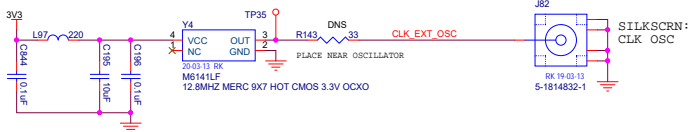
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TERMINATIONS  
CLOSE TO U58



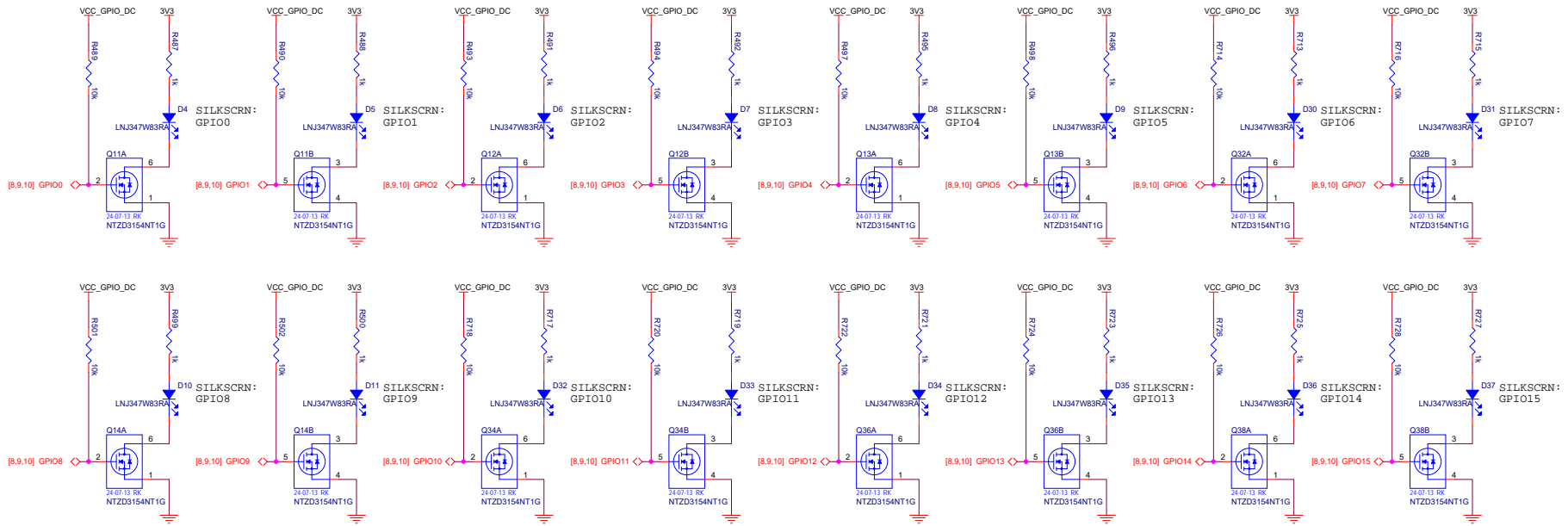
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DESIGN	TITLE	
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DRAWN	SUBTITLE	
DB	PLL Output Clocks	
CHECK	DRAWING NUMBER	REVISION
DB	SK-10280-01	1.2
	RELEASE DATE	SHEET
	27 October 2016	11 OF 16



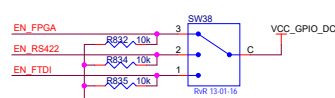
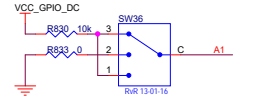
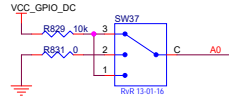
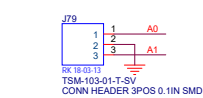
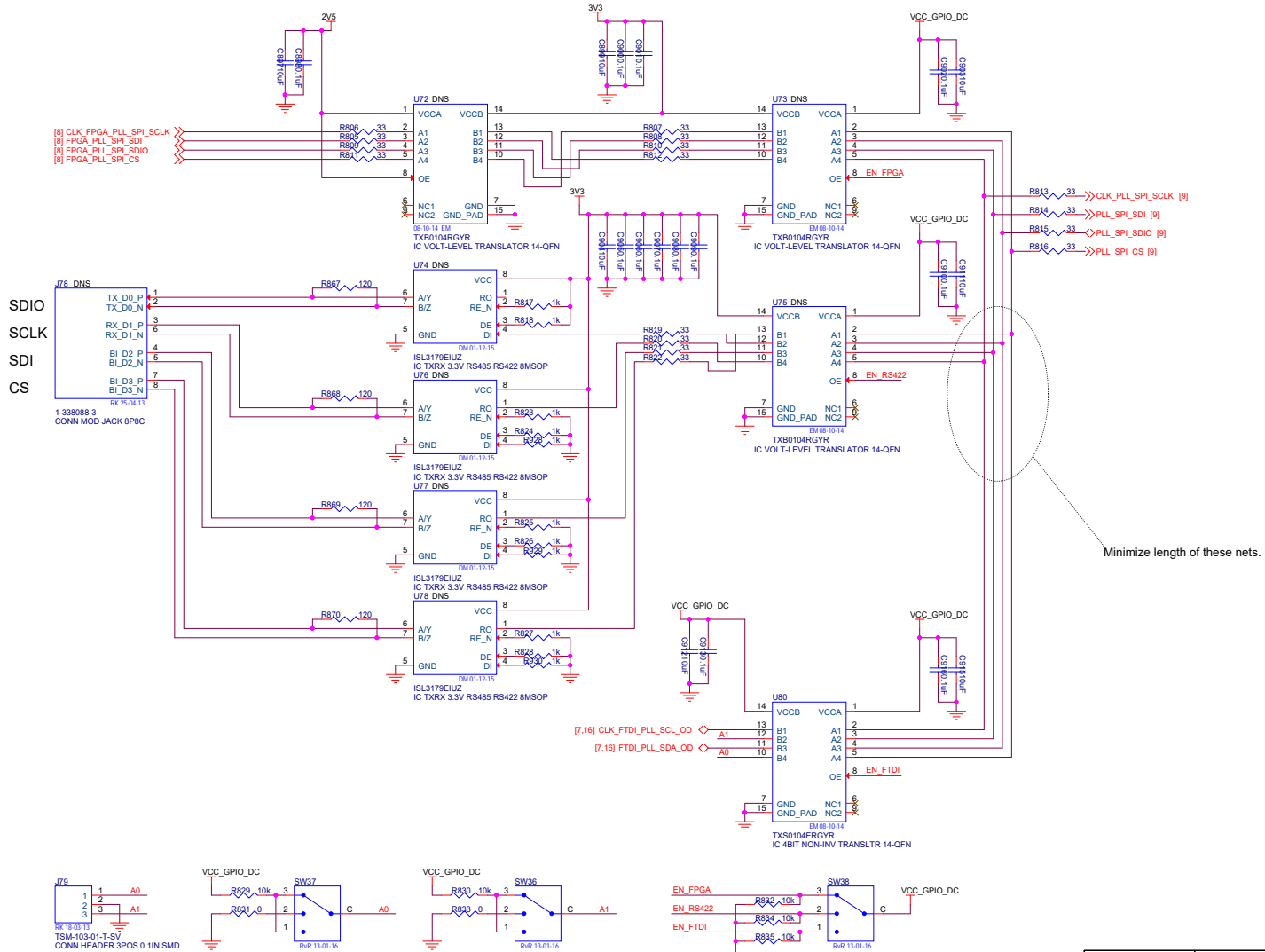
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DRAWN	SUBTITLE <b>PLL Power</b>		
RK	DRAWING NUMBER <b>SK-10280-01</b>		REVISION <b>1.2</b>
CHECK	RELEASE DATE <b>27 October 2016</b>		SHEET <b>12 OF 16</b>
DB			



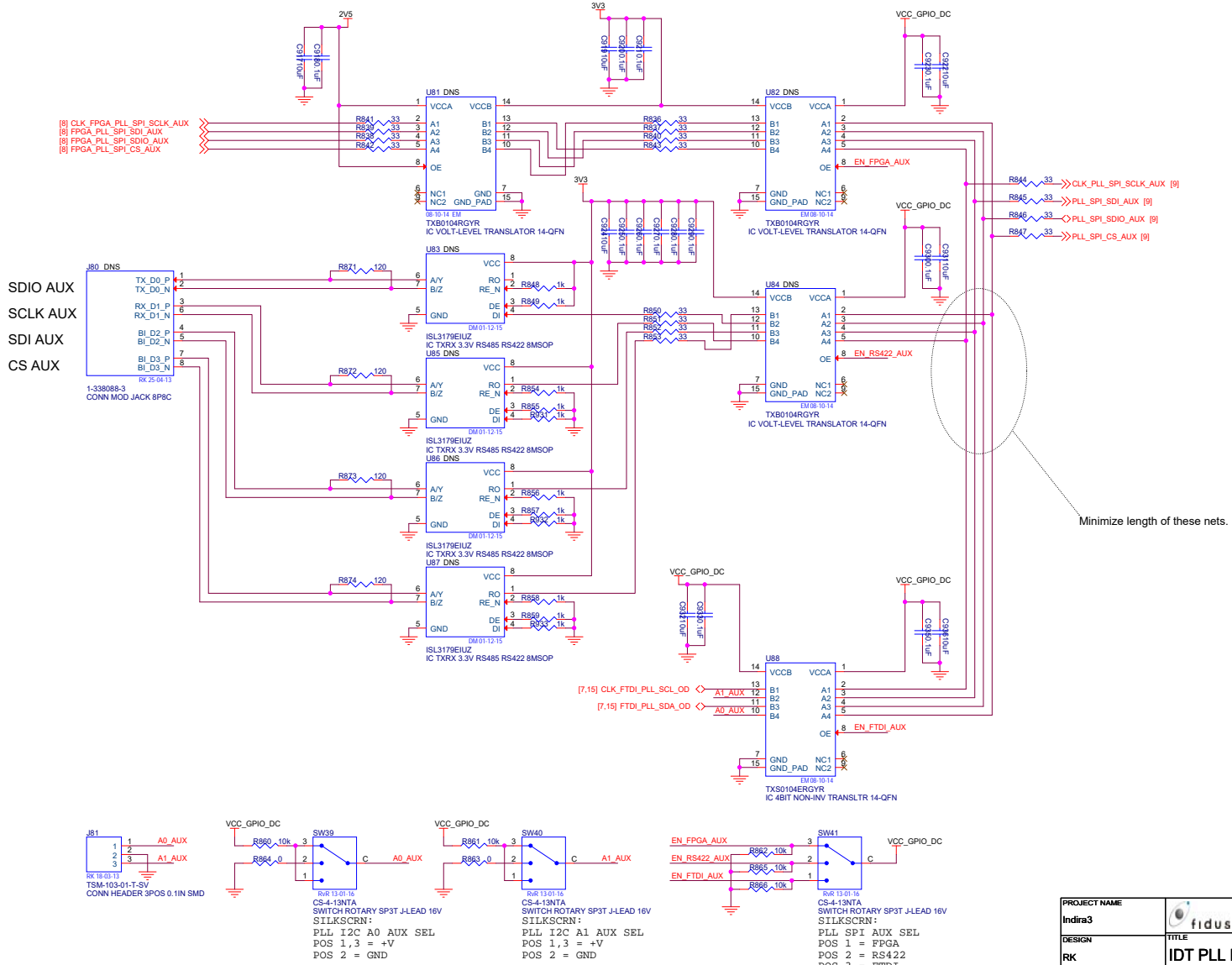
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RK		DRAWING NUMBER SK-10280-01	
CHECK		REVISION 1.2	
DB		RELEASE DATE 27 October 2016	
		SHEET 13 OF 16	



PROJECT NAME		Fidus Systems	
Indira3	375 Terry Fox Drive, Ottawa, ON K2K 0J8		
DESIGN	TITLE		
RK	IDT PLL BGA Chip Carrier		
DRAWN	SUBTITLE		
RK	GPIO LEDs		
CHECK	DRAWING NUMBER	REVISION	
DB	SK-10280-01	1.2	
	RELEASE DATE	SHEET	
	27 October 2016	14 OF 16	



PROJECT NAME	Fidus Systems	
Indra3	375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN	TITLE	
RK	IDT PLL BGA Chip Carrier	
DRAWN	SUBTITLE	
RK	PLL SPI Select	
CHECK	DRAWING NUMBER	REVISION
DB	SK-10280-01	1.2
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	27 October 2016	15 OF 16

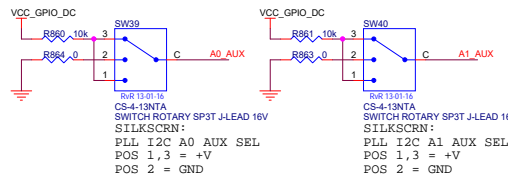


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SDIO AUX  
 SCLK AUX  
 SDI AUX  
 CS AUX

1-338088-3  
 RK25-0413  
 CONN MOD JACK 8P8C

J81  
 RK18-0313  
 TSM-103-01-T-SV  
 CONN HEADER 3POS 0.1IN SMD



PROJECT NAME	Fidus Systems	
Indra3	375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN	TITLE	
RK	IDT PLL BGA Chip Carrier	
DRAWN	SUBTITLE	
RK	PLL AUX SPI Select	
CHECK	DRAWING NUMBER	REVISION
DB	SK-10280-01	1.2
	RELEASE DATE	SHEET
	27 October 2016	16 OF 16