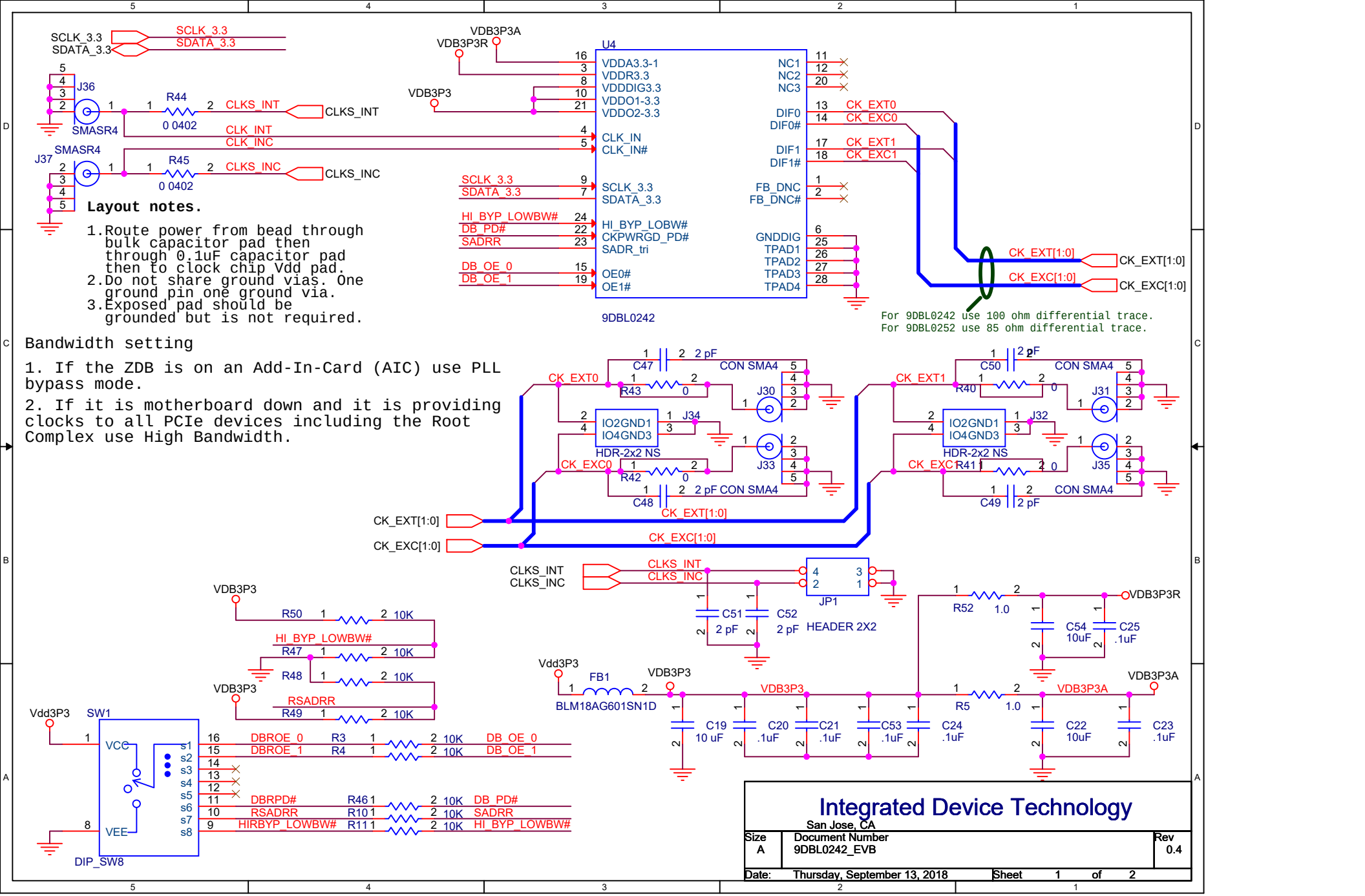
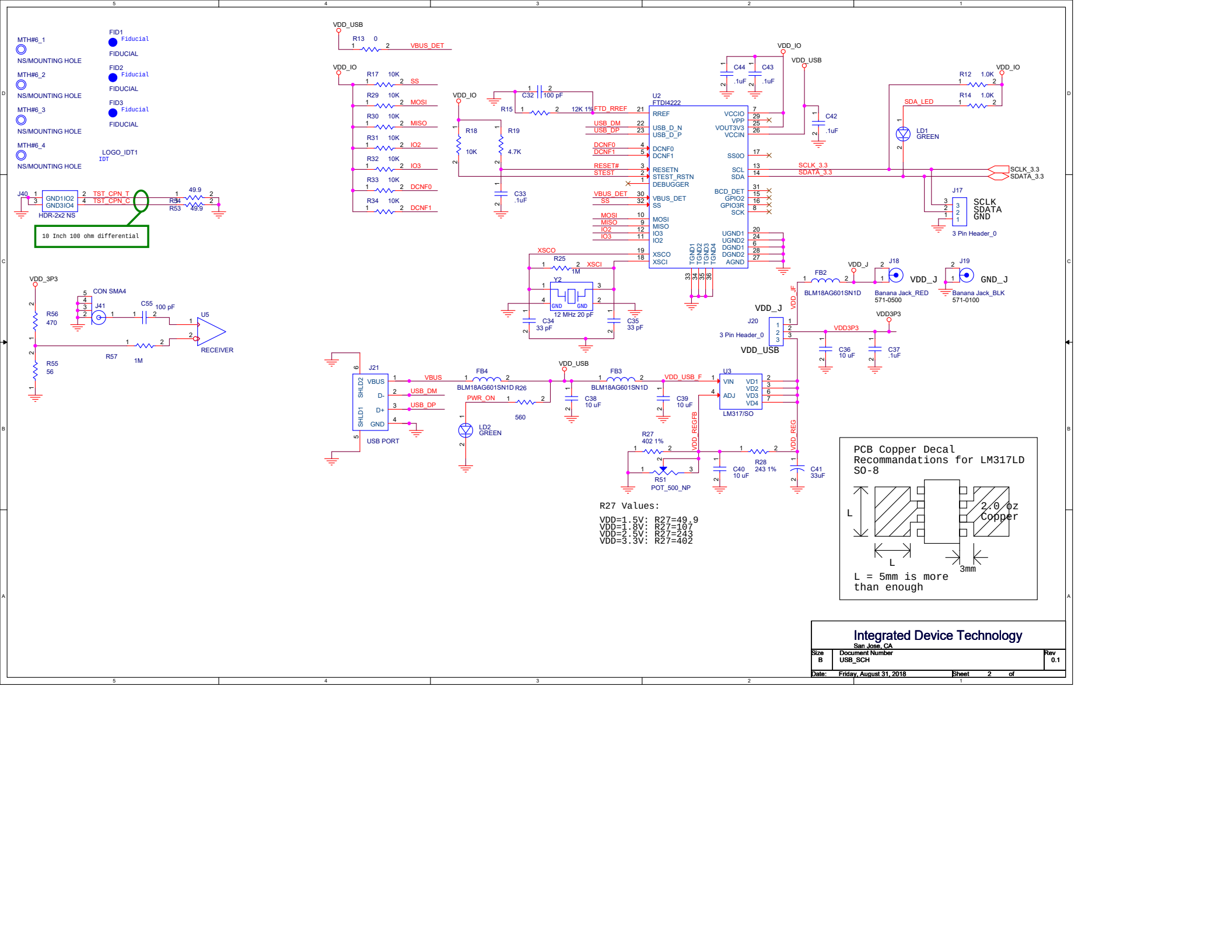

SCLK_3.3
SDATA_3.3
J36
SMASR4
R44
0 0402
CLKS_INT
CLK_INT
CLK_INC
J37
R45
CLKS_INC
Layout notes.
1.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
2.Do not share ground vias. One ground pin one ground via.
3.Exposed pad should be grounded but is not required.
VDB3P3A
VDB3P3R
VDB3P3
U4
VDDA3.3-1
VDDR3.3
VDDDIG3.3
VDDO1-3.3
VDDO2-3.3
CLK_IN
CLK_IN#
SCLK_3.3
SDATA_3.3
HI_BYP_LOWBW#
DB_PD#
SADRR
DB_OE_0
DB_OE_1
OE0#
OE1#
NC1
NC2
NC3
DIF0
DIF0#
DIF1
DIF1#
FB_DNC
FB_DNC#
GNDDIG
TPAD1
TPAD2
TPAD3
TPAD4
CK_EXT0
CK_EXC0
CK_EXT1
CK_EXC1
CK_EXT[1:0]
CK_EXC[1:0]
9DBL0242
For 9DBL0242 use 100 ohm differential trace.
For 9DBL0252 use 85 ohm differential trace.
Bandwidth setting
1. If the ZDB is on an Add-In-Card (AIC) use PLL bypass mode.
2. If it is motherboard down and it is providing clocks to all PCIe devices including the Root Complex use High Bandwidth.
C47
C48
C49
C50
R43
R42
R40
R41
J30
J31
J32
J33
J34
J35
IO2GND1
IO4GND3
HDR-2x2 NS
CON SMA4
2 pF
CLKS_INT
CLKS_INC
JP1
HEADER 2X2
C51
C52
R52
R5
C54
C25
C19
C20
C21
C53
C24
C22
C23
FB1
BLM18AG601SN1D
Vdd3P3
10 uF
.1uF
10uF
1.0
R50
R47
R48
R49
HI_BYP_LOWBW#
RSADRR
10K
SW1
VCC
VEE
DIP_SW8
DBROE_0
DBROE_1
DBRPD#
RSADRR
HIRBYP_LOWBW#
R3
R4
R46
R10
R11
DB_OE_0
DB_OE_1
DB_PD#
SADRR
HI_BYP_LOWBW#
Integrated Device Technology
San Jose, CA
Size
A
Document Number
9DBL0242_EVB
Rev
0.4
Date:
Thursday, September 13, 2018
Sheet
1
of
2


MTH#6_1
NS/MOUNTING HOLE
MTH#6_2
NS/MOUNTING HOLE
MTH#6_3
NS/MOUNTING HOLE
MTH#6_4
NS/MOUNTING HOLE
FID1
Fiducial
FIDUCIAL
FID2
Fiducial
FIDUCIAL
FID3
Fiducial
FIDUCIAL
LOGO_IDT1
IDT
J40
GND1IO2
GND3IO4
HDR-2x2 NS
TST_CPN_T
TST_CPN_C
49.9
R54
R53
10 Inch 100 ohm differential
VDD_3P3
CON SMA4
J41
C55
100 pF
U5
RECEIVER
R56
470
R55
56
R57
1M
VDD_USB
R13 0
VBUS_DET
VDD_IO
R17 10K
R29 10K
R30 10K
R31 10K
R32 10K
R33 10K
R34 10K
SS
MOSI
MISO
IO2
IO3
DCNF0
DCNF1
R18
10K
R19
4.7K
C33
.1uF
C32
100 pF
R15
12K 1%
FTD_RREF
U2
FTDI4222
RREF
USB_D_N
USB_D_P
DCNF0
DCNF1
RESETN
STEST_RSTN
DEBUGGER
VBUS_DET
SS
MOSI
MISO
IO2
IO3
XSCO
XSCI
VCCIO
VPP
VOUT3V3
VCCIN
SS0O
SCL
SDA
BCD_DET
GPIO2
GPIO3R
SCK
UGND1
UGND2
DGND1
DGND2
AGND
TGND1
TGND2
TGND3
TGND4
C44
.1uF
C43
.1uF
C42
.1uF
R12 1.0K
R14 1.0K
SDA_LED
LD1
GREEN
SCLK_3.3
SDATA_3.3
J17
SCLK
SDATA
GND
3 Pin Header_0
R25
1M
Y2
12 MHz 20 pF
C34
33 pF
C35
33 pF
FB2
BLM18AG601SN1D
VDD_J
J18
Banana Jack_RED
571-0500
J19
Banana Jack_BLK
571-0100
GND_J
J20
3 Pin Header_0
VDD_JF
VDD3P3
C36
10 uF
C37
.1uF
J21
USB PORT
VBUS
D-
D+
GND
SHLD1
SHLD2
FB4
BLM18AG601SN1D
R26
560
PWR_ON
LD2
GREEN
FB3
BLM18AG601SN1D
C38
10 uF
VDD_USB_F
U3
LM317/SO
VIN
ADJ
VD1
VD2
VD3
VD4
C39
10 uF
VDD_REGFB
VDD_REG
R27
402 1%
R51
POT_500_NP
R28
243 1%
C40
10 uF
C41
33uF
R27 Values:
VDD=1.5V: R27=49.9
VDD=1.8V: R27=107
VDD=2.5V: R27=243
VDD=3.3V: R27=402
PCB Copper Decal
Recommandations for LM317LD
SO-8
L
2.0 oz
Copper
L
3mm
L = 5mm is more
than enough
Integrated Device Technology
San Jose, CA
Size
B
Document Number
USB_SCH
Rev
0.1
Date:
Friday, August 31, 2018
Sheet
2
of