

IDT CLOCKS FOR SMPTE AND XILINX® 7 SERIES FPGAS

INTRODUCTION

SMPTE (Society of Motion Picture & Television Engineering) is an internationally recognized standards body whose governing specifications include that for the high-speed serial physical interfaces for transmission of digital TV. Commonly called SDI (Serial Data Interface), a summary of these standards is detailed in Table 1.

Standard	Name	Bitrates	Display Formats
SMPTE 259M	"Standard Definition" SD-SDI	270 Mbps (4:3) 360 Mbps (16:9)	525i/59.94 [NTSC], 625i/50[PAL], 480i, 576i
SMPTE 344M	"Enhanced Definition" ED-SDI	540 Mbps	525i/59.94 [NTSC], 625i/50[PAL], 480p, 576p
SMPTE 292M	"High Definition" HD-SDI	1.485 Gbps 1.485/1.001 Gbps	720p, 1080i
SMPTE 372M	"Dual Link" HD-SDI	2.970 Gbps 2.970/1.001 Gbps	1080p
SMPTE 424M	"3 gig" 3G-SDI	2.970 Gbps 2.970/1.001 Gbps	1080p

Table 1: SMPTE SDI Standards

SMPTE 424, also known as 3G-SDI, has very stringent eye jitter requirements for the high performance 3 Gbps SerDes in order to meet the desired Bit Error Rate (BER).

- Timing Jitter Specification
 - 2.0 UI max peak to peak (10 Hz to 100 KHz)
- Alignment Jitter Specification
 - 0.3 UI max peak to peak (100 KHz to 297 MHz); 0.2 UI recommended

A unit interval (UI) is defined as the time between two adjacent signal transitions, which is the reciprocal of clock frequency, and is 336.7 ps for 3G-SDI serial digital (SMPTE 424M).

The latest Xilinx® 7 Series FPGAs are commonly used in SMPTE applications because of their integrated high performance GTX/GTH/GTP transceivers. But, in order to meet the SMPTE 424 eye jitter specifications, Xilinx specifies very tight dBc/Hz phase noise requirements for the reference clock used to drive these SerDes..

To further exacerbate the technical challenge, many broadcast video designs need to support both NTSC and PAL HDTV standards which means that both 148.5 MHz and 148.5/(1.001) MHz reference clocks need to be simultaneously supported.

Additionally, the latest trend of broadcast video products supporting Video-Over-IP may also need to support 10GE PHYs where an additional 156.25 MHz reference clock is typically needed. And, if the same Xilinx 7 Series GTX/GTH/GTP transceivers are also used to implement the 10 Gbps SerDes, the very tight dBc/Hz phase noise requirements come into play once again.

These non-integer related clock frequencies (148.5 MHz, 148.351648 MHz, 156.25MHz), combined with very tight phase noise requirements for each, mean that an integrated clock solution is no trivial task. IDT's Universal Frequency Translator™ (UFT™) family of high-end PLLs can synthesize all of these high-performance clocks in a single device. Also, the UFT family has the advanced features needed to implement a more complex Genlock implementation. Both of these use cases using IDT's UFT are detailed in this technical brief.

XILINX 7 SERIES PHASE NOISE REQUIREMENTS

10GE and SMPTE 424 serial interface standards specify the total eye jitter, and do not allocate a budget specific to the reference clock used to drive the SerDes. As a result, board designers are forced to use the reference clock jitter specification provided by the SerDes vendor. [Xilinx Action Record \(AR\) # 44549](#) specifies the 7 Series reference clock phase noise.

Figure 1 is a summary of this specification for both QPLL and CPLL internal clock multiplying PLLs that are used for generating the internal SerDes transmit and receive clocks. Exceeding these limits for the reference clock can adversely impact the transmit jitter and receive jitter tolerance of the GTX/GTH/GTP transceivers.

REFCLK (MHz)	QPLL (LC Tank Oscillator PLL) - Phase Noise (dBc) -			CPLL (Ring Oscillator PLL) - Phase Noise (dBc) -		
	@10 KHz	@100 KHz	@1 MHz	@10 KHz	@100 KHz	@1 MHz
100	-126	-130	-134	-126	-132	-136
125	-123	-129	-133	-123	-131	-135
156.25	-122	-127	-132	-121	-129	-133
250	-119	-126	-131	-119	-126	-132
312.5	-115	-124	-130	-116	-124	-131
625	-110	-116	-120	-110	-119	-127

156.25 MHz }
148.5 MHz }
148.5/(1.001) MHz }

Figure 1: Xilinx 7 Series Phase Noise Requirements

A reference clock used to drive a 7 Series GTX/GTH/GTP transceiver must meet these dBc/Hz specs for all three carrier frequency offsets (10 KHz, 100 KHz, and 1 MHz), regardless of the line rate. Note that if not listed, then the designer must use the phase noise mask of the nearest reference clock frequency. Xilinx provides specifications for these 3 offset frequencies because of the 7 Series internal PLL bandwidth. Lower and higher offset frequencies have significant margin and so are not specified.

Some clock device datasheets provide dBc/Hz phase noise specifications at these frequency offsets. But, the designer is encouraged to have phase noise plots generated for their specific application as results can vary significantly depending on the clock configuration needed. The phase noise "mask" can then be plotted on the same phase noise plot by connecting the 3

points dictated by AR# 44549. If the phase noise plot is below the mask, then the designer can be confident that the reference clock will be okay. If not, then additional jitter on the transmitted data can be expected and may result in a higher BER.

IDT CLOCK SOLUTIONS

IDT's Universal Frequency Translator™ (UFT™) family of clock devices has the performance required for Xilinx 7 Series reference clock applications. Figure 2 details a typical phase noise plot for a 156.25 MHz output clock generated by an IDT UFT clock device. As demonstrated in Figure 2, the phase noise plot lies comfortably below the phase noise mask defined in AR# 44549.

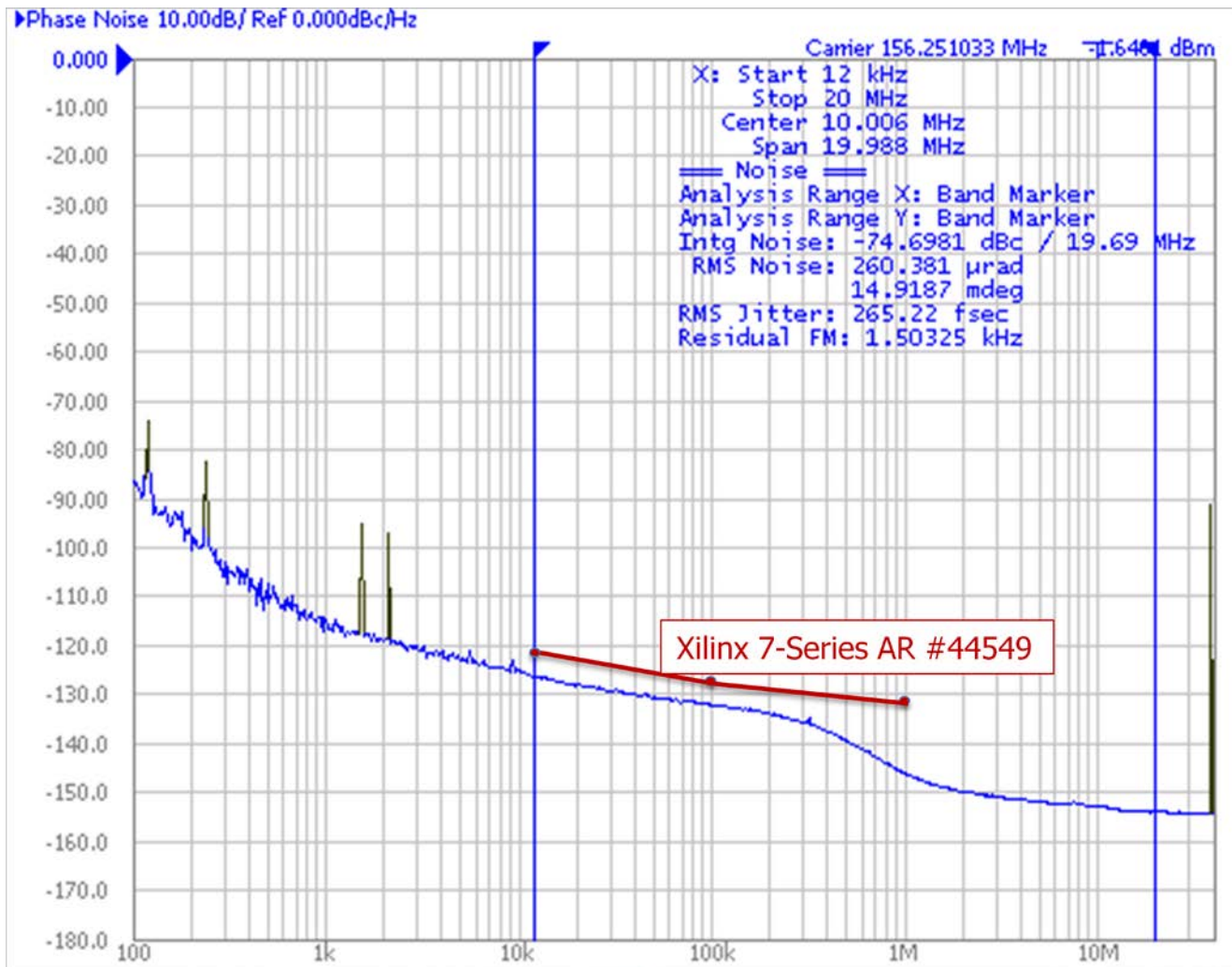


Figure 2: UFT3G 156.25MHz "typical" PN Plot, with AR #44549 Phase Noise Mask

Synthesis Use Case with 8T49N241

The UFT family can be used as a high performance synthesizer, requiring only a simple fundamental mode parallel resonant XTAL as its input reference. Figure 3 details one such use case with IDT's [8T49N241](#).

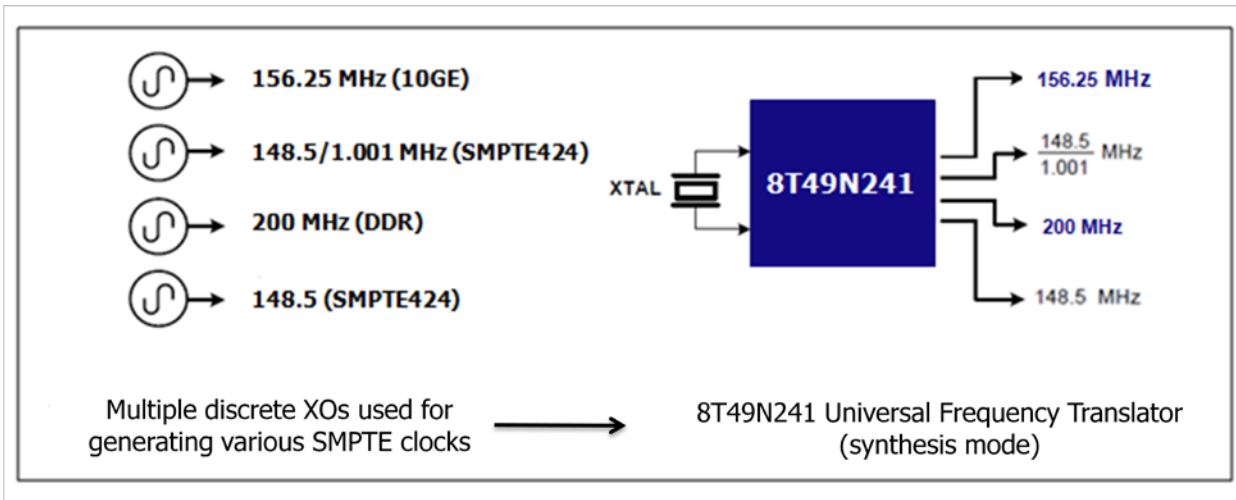


Figure 3: Example 8T49N241 Synthesis Use Case

For this use case the 8T49N241 is being used as a high-performance four output synthesizer. Figure 3a is a screen capture of the corresponding Timing Commander™ GUI configured for this same use case. The combination of a fractional-feedback PLL and a mix of integer and fractional output dividers allow the 8T49N241 to generate all of these output frequencies with 0 ppb additive synthesis error. And the measured phase noise performance of the 10GE and SMPTE 424 clocks meets the 7 Series requirement.

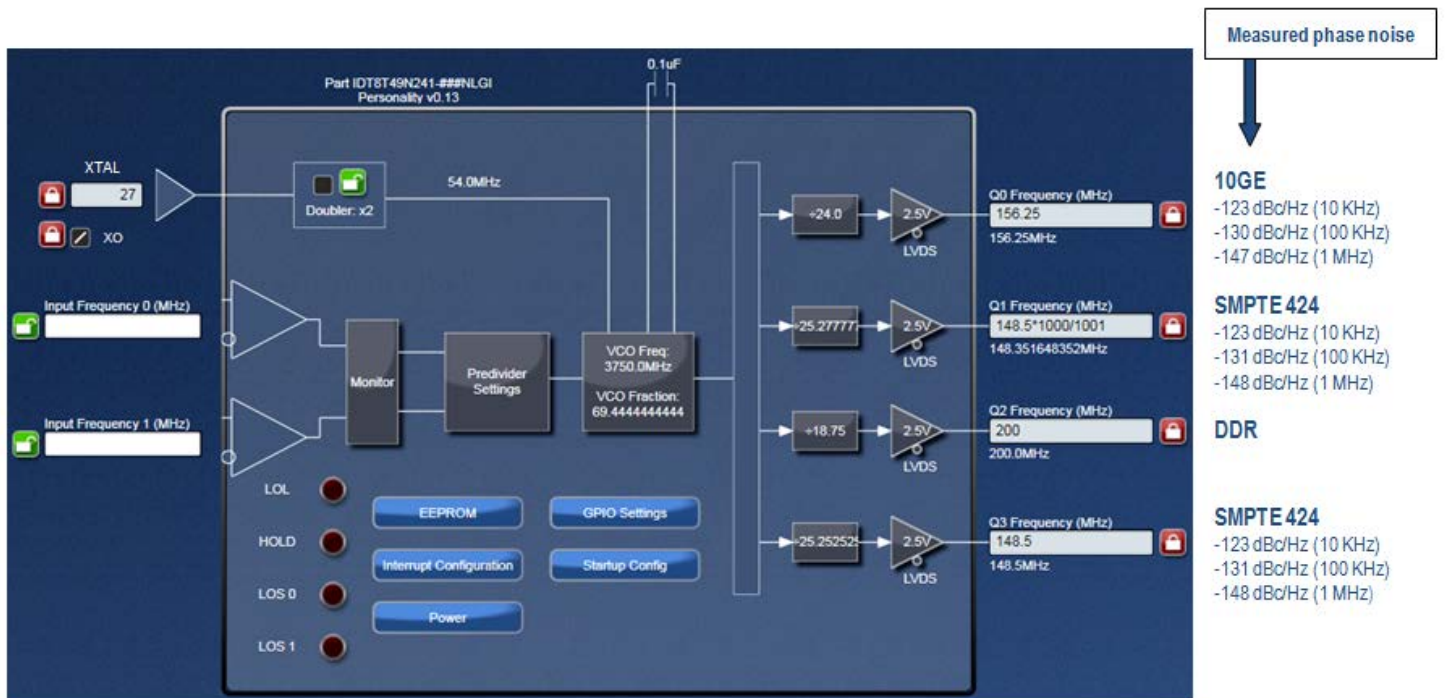


Figure 3a: Corresponding 8T49N241 Timing Commander GUI Configuration

Genlock Use Case with 8T49N287

The UFT family can also be used as a high performance input clock jitter attenuator and frequency translator required for a traditional SMPTE Genlock application. Figure 4 details one such use case with the [8T49N287](#).

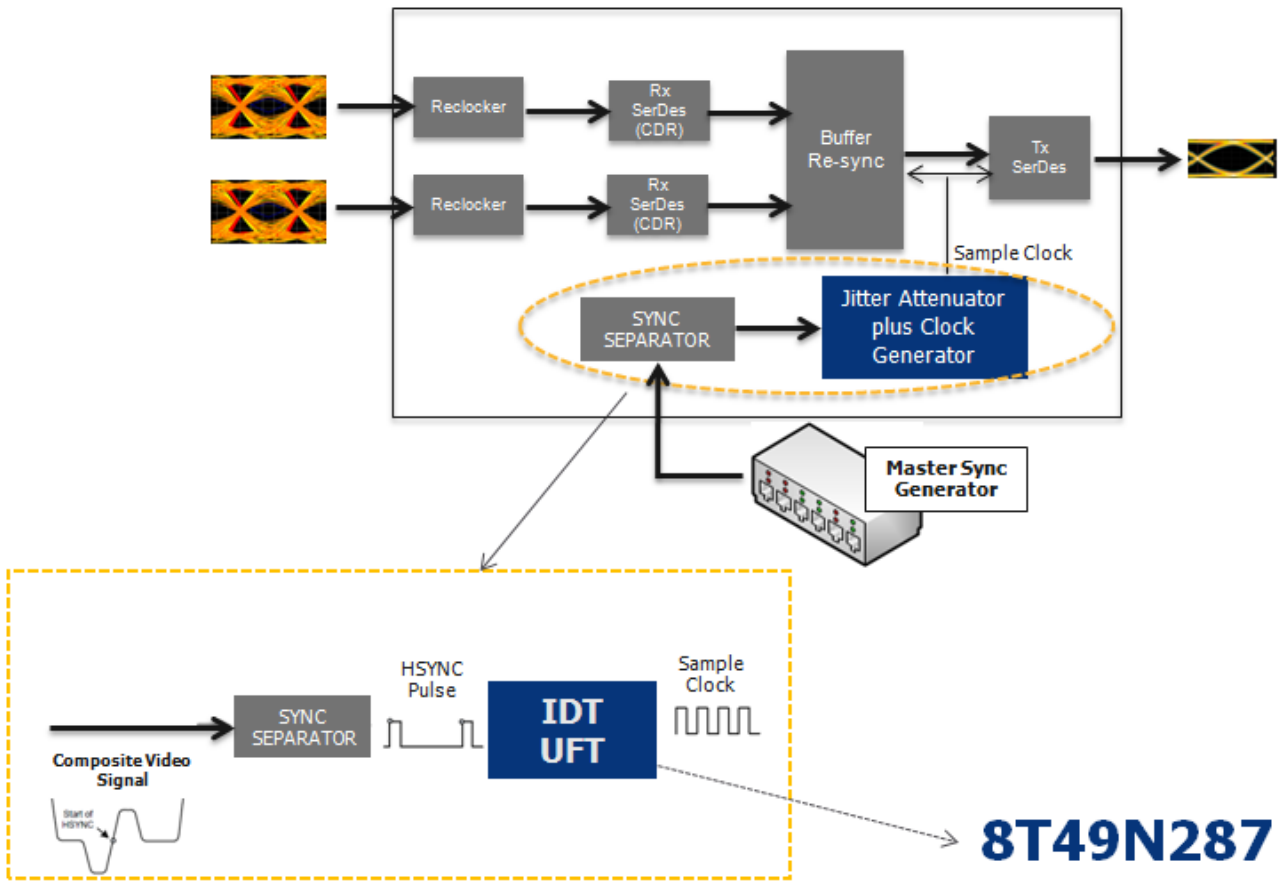


Figure 4: Example 8T49N287 Genlock Use Case

Figure 4a details the dual PLL architecture of the UFT. For this use case, the 8T49N287 device accepts an HSYNC pulse from the sync separator, and then uses the internal Digital PLL to compare the reference to the scaled output of the VCO based APLL, also internal to the device. The output of the DPLL is then used to steer the fractional feedback divider of the APLL. The end result is that the high performance output of the APLL is edge aligned with the HSYNC reference, and any input jitter from the HSYNC reference is eliminated. Note that the four output 8T49N241 also has this same capability.

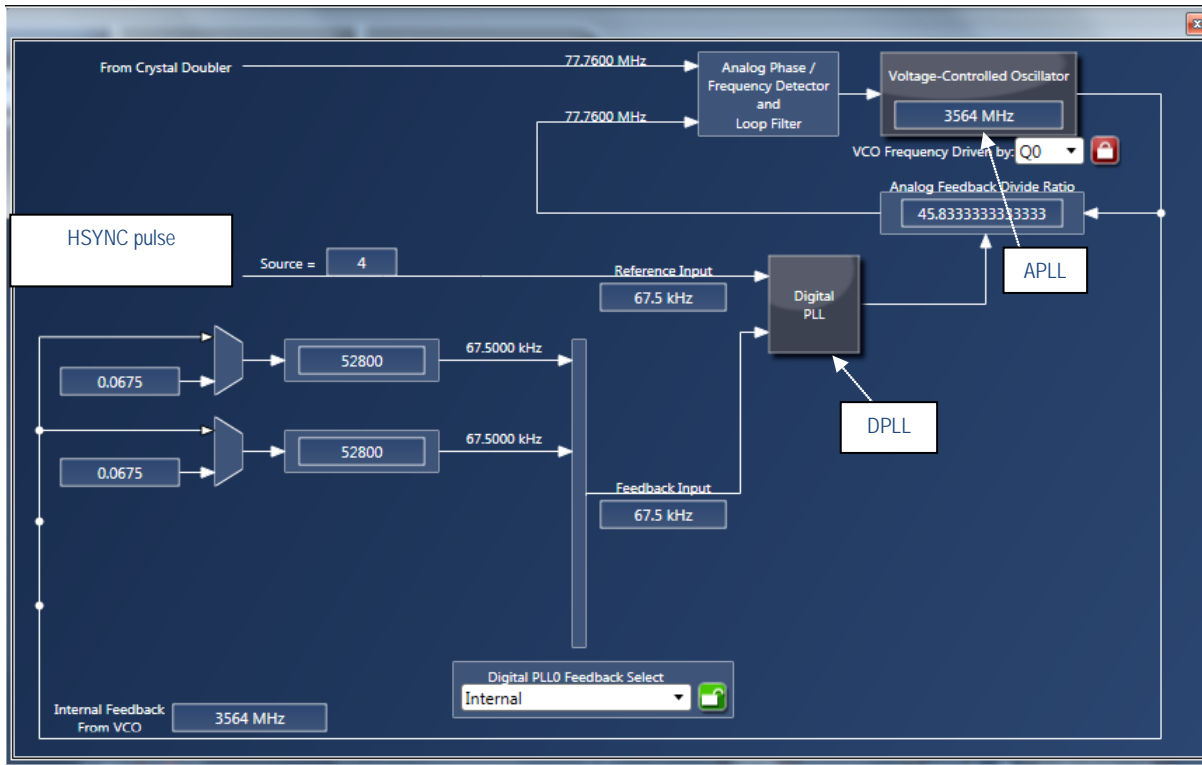


Figure 4a: Jitter Attenuation and Frequency Translation with Dual PLL Structure of UFT

Figure 4b is a screen capture of the corresponding Timing Commander GUI configured for this same use case. Once again, the combination of fractional-feedback PLLs and a mix of integer and fractional output dividers allow the 8T49N287 to use its 8 outputs to generate all of these frequencies with 0ppb additive synthesis error. And the measured phase noise performance of the 10GE and SMPTE 424 clocks meets the 7 Series requirement.

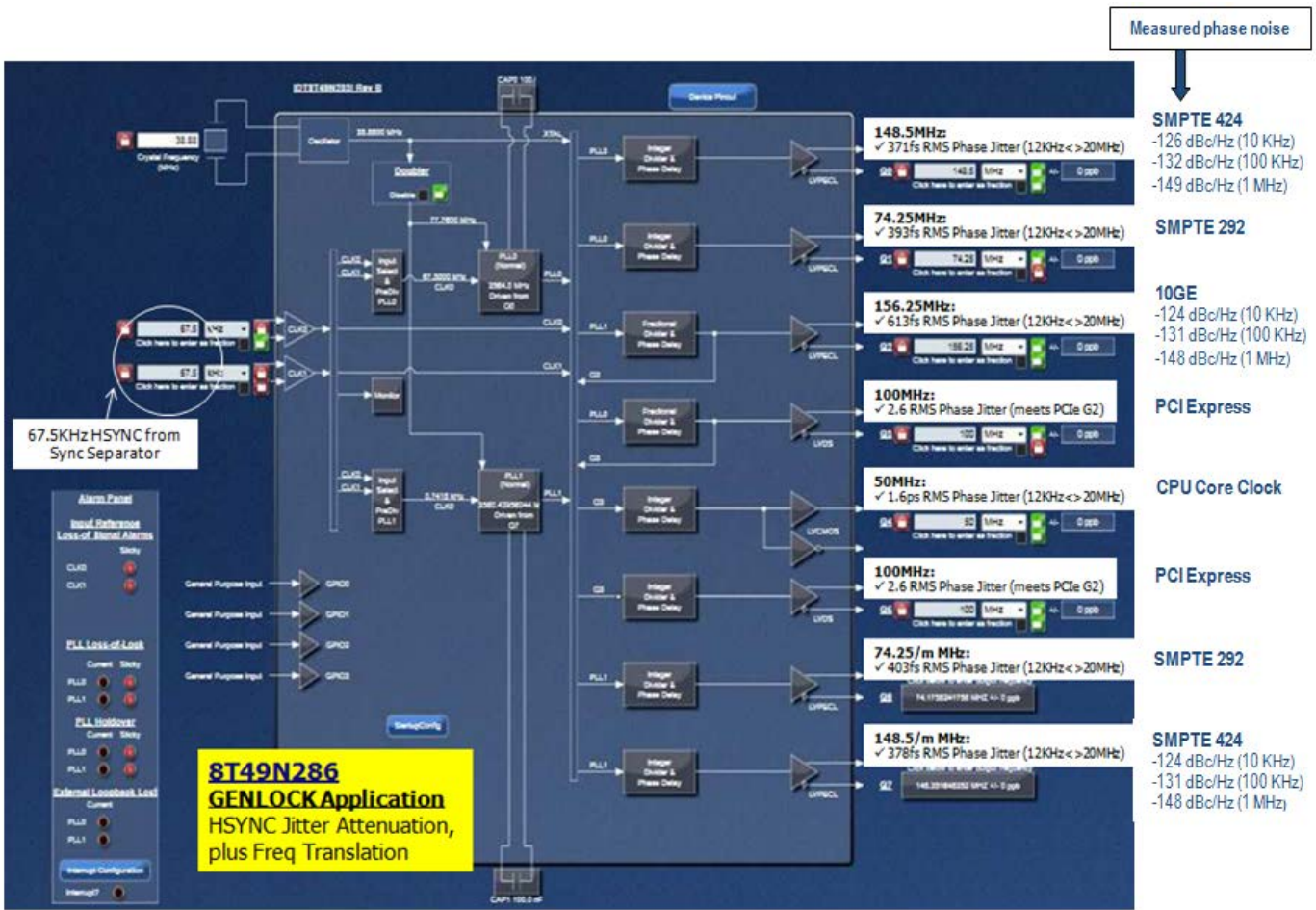


Figure 4b: Corresponding 8T49N287 Timing Commander GUI Configuration

CONCLUSION

The IDT family of UFT devices can generate the multiple non-integer related clock frequencies needed for today's SMPTE compliant multi-rate broadcast video equipment. Furthermore, the high performance APLL design implemented in the UFT meets the stringent phase noise requirements of the Xilinx 7 Series GTX/GTH/GTP transceivers. And, the UFT can be used in simple synthesis only use cases, or as a jitter attenuator plus frequency translator typically needed for traditional Genlock applications

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