

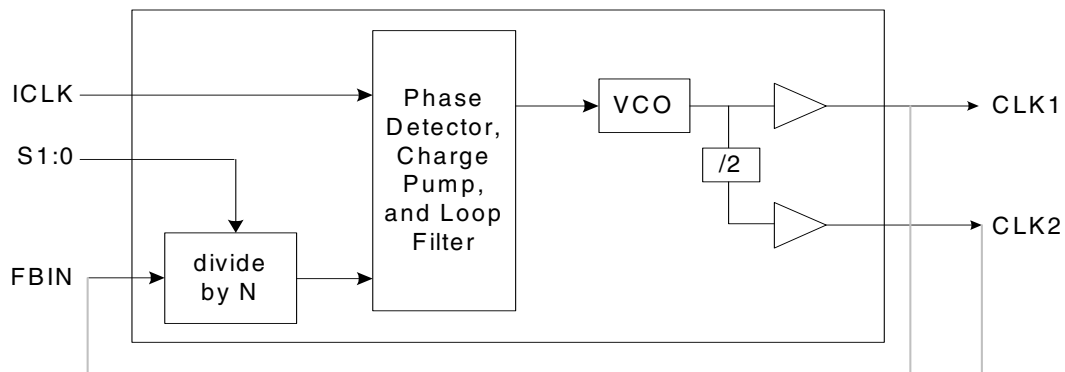
**MULTIPLIER AND ZERO DELAY BUFFER**
**MK2302-01**
**Description**

The MK2302-01 is a high performance Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. The chip is part of IDT's ClockBlocks™ family and was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both output clocks, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other output.

The MK2302-01 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to graphics/video. By allowing off-chip feedback paths, the device can eliminate the delay through other devices.

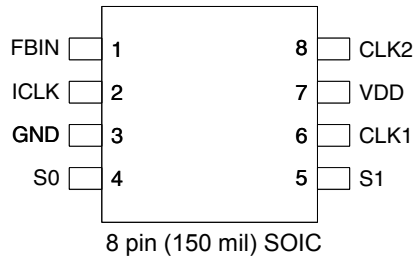
**Features**

- 8-pin SOIC package
- Pb (lead) free package
- Low input to output skew of 250 ps max
- Absolute jitter  $\pm 500$  ps
- Propagation Delay  $\pm 350$  ps
- Ability to choose between different multipliers from 0.5X to 16X
- Output clock frequency up to 168 MHz at 3.3 V
- Can recover degraded input clock duty cycle
- Output clock duty cycle of 45/55
- Full CMOS clock swings with 25mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature version available

**Block Diagram**


External feedback can come from CLK1 or CLK2 (see table on page 2)

## Pin Assignment



## Clock Multiplier Decoding Table 1

(Multiplies Input clock by shown amount)

| FBIN | S1 | S0 | CLK1      | CLK2     |
|------|----|----|-----------|----------|
| CLK1 | 0  | 0  | 2 X ICLK  | ICLK     |
| CLK1 | 0  | 1  | 4 X ICLK  | 2 X ICLK |
| CLK1 | 1  | 0  | ICLK      | ICLK/2   |
| CLK1 | 1  | 1  | 8 X ICLK  | 4 X ICLK |
| CLK2 | 0  | 0  | 4 X ICLK  | 2 X ICLK |
| CLK2 | 0  | 1  | 8 X ICLK  | 4 X ICLK |
| CLK2 | 1  | 0  | 2 X ICLK  | ICLK     |
| CLK2 | 1  | 1  | 16 X ICLK | 8 X ICLK |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description                                                      |
|------------|----------|----------|----------------------------------------------------------------------|
| 1          | FBIN     | Input    | Feedback clock input.                                                |
| 2          | ICLK     | Input    | Reference clock input.                                               |
| 3          | GND      | Power    | Connect to ground.                                                   |
| 4          | S0       | Input    | Select 0 for output clock per decoding table above. Pull-up.         |
| 5          | S1       | Input    | Select 1 for output clock per decoding table above. Pull up.         |
| 6          | CLK1     | Output   | Clock output per table above.                                        |
| 7          | VDD      | Power    | Connect to +3.3 V or +5.0 V.                                         |
| 8          | CLK2     | Output   | Clock output per table above. Low skew divide by two of pin 6 clock. |

## External Components

The MK2302-01 requires a 0.01 $\mu$ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the part to minimize lead inductance. No external power supply filtering is required for this device. A 33 $\Omega$  series terminating resistor can be used next to each output pin.

Using CLK1 as the feedback will always result in synchronized rising edges between ICLK and CLK1. However, the CLK2 could be a falling edge compared with ICLK. IDT recommends using CLK2 feedback whenever possible. This will synchronize the rising edges of all three clocks.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2302-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating              |
|-------------------------------|---------------------|
| Supply Voltage, VDD           | 7 V                 |
| All Inputs and Outputs        | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -55 to 125° C       |
| Storage Temperature           | -65 to +150° C      |
| Junction Temperature          | 125° C              |
| Power Dissipation             | 0.5 W               |

## Recommended Operation Conditions

| Parameter                                         | Min.  | Typ. | Max.  | Units |
|---------------------------------------------------|-------|------|-------|-------|
| Ambient Operating Temperature (commercial)        | 0     |      | +70   | °C    |
| Ambient Operating Temperature (industrial)        | -40   |      | +85   | °C    |
| Power Supply Voltage (measured in respect to GND) | +4.5  | +5.0 | +5.5  | V     |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V     |

## DC Electrical Characteristics

VDD = 3.3 V  $\pm$ 5%, Ambient Temperature 0 to +70°C or -40°C to 85°C

| Parameter                       | Symbol          | Conditions               | Min.    | Typ.     | Max. | Units |
|---------------------------------|-----------------|--------------------------|---------|----------|------|-------|
| Operating Voltage               | VDD             |                          | 3.15    |          | 3.45 | V     |
| Operating Current               | IDD             |                          |         | 20       |      | ma    |
| Input High Voltage              | V <sub>IH</sub> | ICLK, FBIN               | 2       |          |      | V     |
| Input Low Voltage               | V <sub>IL</sub> | ICLK, FBIN               |         |          | 0.8  | V     |
| Input High Voltage              | V <sub>IH</sub> | S0, S1                   | VDD-0.5 |          |      | V     |
| Input Low Voltage (mid-level)   | V <sub>IM</sub> | S0, S1                   |         | VDD/2    |      | V     |
| Input Low Voltage               | V <sub>IL</sub> | S0, S1                   |         |          | 0.5  | V     |
| Output High Voltage (CMOS High) | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA  | VDD-0.4 |          |      | V     |
| Output High Voltage             | V <sub>OH</sub> | I <sub>OH</sub> = -12 mA | 2.4     |          |      | V     |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>OL</sub> = 12 mA  |         |          | 0.4  | V     |
| Short Circuit Current           | I <sub>OS</sub> | Each output              |         | $\pm$ 70 |      | mA    |
| Input Capacitance               | C <sub>IN</sub> | S0, S1                   |         | 5        |      | pF    |

VDD = 5 V  $\pm$ 10%, Ambient Temperature 0 to +70°C or -40°C to 85°C

| Parameter                       | Symbol          | Conditions               | Min.    | Typ.      | Max. | Units |
|---------------------------------|-----------------|--------------------------|---------|-----------|------|-------|
| Operating Voltage               | VDD             | 5V                       | 4.5     |           | 5.5  | V     |
| Operating Current               | IDD             |                          |         | 30        |      | ma    |
| Input High Voltage              | V <sub>IH</sub> | ICLK, FBIN               | 2       |           |      | V     |
| Input Low Voltage               | V <sub>IL</sub> | ICLK, FBIN               |         |           | 0.8  | V     |
| Input High Voltage              | V <sub>IH</sub> | S0, S1                   | VDD-0.5 |           |      | V     |
| Input Low Voltage (mid-level)   | V <sub>IM</sub> | S0, S1                   |         | VDD/2     |      | V     |
| Input Low Voltage               | V <sub>IL</sub> | S0, S1                   |         |           | 0.5  | V     |
| Output High Voltage (CMOS High) | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA  | VDD-0.4 |           |      | V     |
| Output High Voltage             | V <sub>OH</sub> | I <sub>OH</sub> = -12 mA | 2.4     |           |      | V     |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>OL</sub> = 12 mA  |         |           | 0.4  | V     |
| Short Circuit Current           | I <sub>OS</sub> | Each output              |         | $\pm$ 100 |      | mA    |
| Input Capacitance               | C <sub>IN</sub> | S0, S1                   |         | 5         |      | pF    |

## AC Electrical Characteristics

VDD = 3.3 V or 5 V  $\pm$ 5%, Ambient Temperature 0 to +70° C or -40° C to 85° C

| Parameter               | Symbol | Conditions                          | Min.                | Typ.    | Max. | Units |
|-------------------------|--------|-------------------------------------|---------------------|---------|------|-------|
| Input Frequency, ICLK   |        | FBIN from CLK/2                     | See table on page 2 |         |      |       |
| Output Clock Frequency  |        | CLK1                                | 10                  |         | 168  | MHz   |
| Output to Output Skew   |        |                                     |                     | 100     | 175  | ps    |
| Input to Output Jitter  |        | 40 - 150 MHz                        |                     |         | 200  | ps    |
| Input Skew              |        | ICLK to FBIN,<br>CLK>30 MHz, Note 1 | -300                |         | 300  | ps    |
|                         |        | ICLK to FBIN,<br>CLK<30 MHz, Note 1 | -600                |         | 600  | ps    |
| Output Clock Rise Time  |        | 0.8 to 2.0 V, Note 2                |                     | 0.8     | 1    | ns    |
| Output Clock Fall Time  |        | 2.0 to 0.8 V, Note 2                |                     | 0.8     | 1    | ns    |
| Output Clock Duty Cycle |        | at VDD/2                            | 40                  | 49 - 51 | 60   | %     |

Note 1: Assumes clocks with same rise time, measured from rising edges at VDD/2.

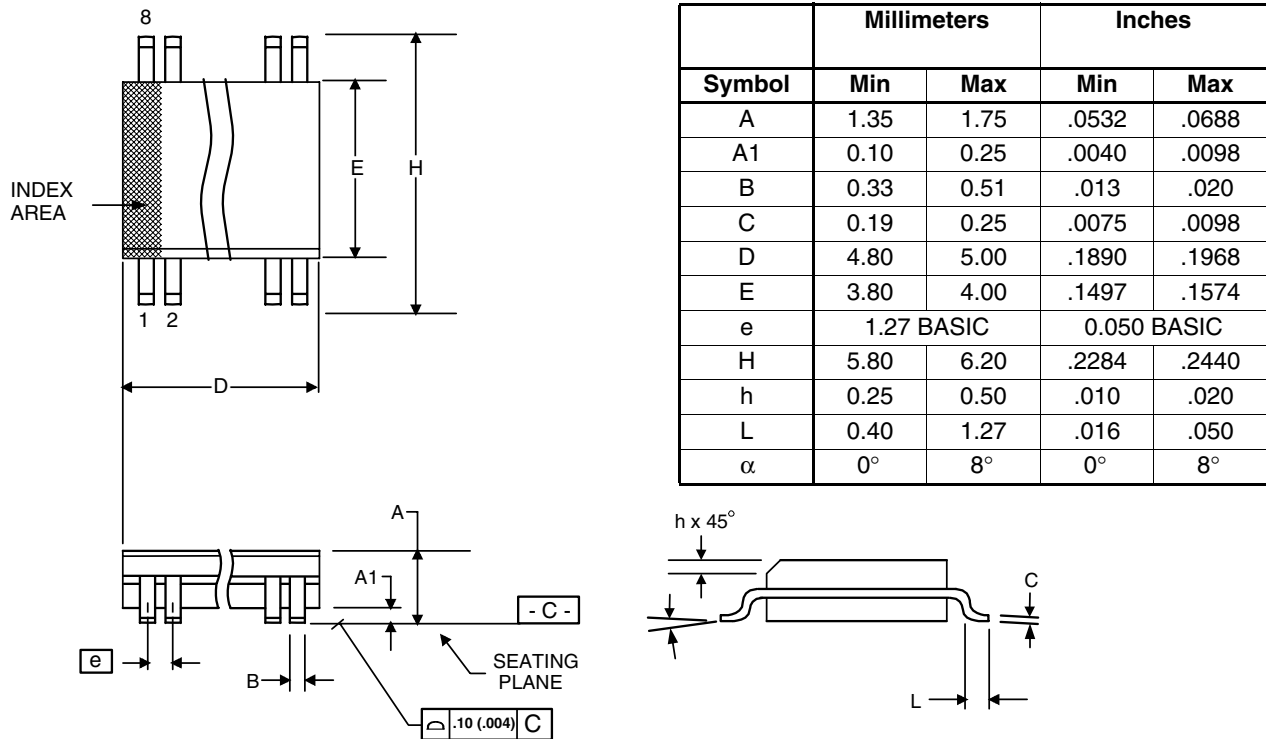
Note 2: Measured with 27 $\Omega$  terminating resistor and 15 pF loads.

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|----------------------------------------|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 150  |      | °C/W  |
|                                        | $\theta_{JA}$ | 1 m/s air flow |      | 140  |      | °C/W  |
|                                        | $\theta_{JA}$ | 3 m/s air flow |      | 120  |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 40   |      | °C/W  |

## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

| Part / Order Number | Marking   | Shipping Pkg  | Package    | Temperature  |
|---------------------|-----------|---------------|------------|--------------|
| MK2302S-01LF        | 230201LF  | Tubes         | 8-pin SOIC | 0 to +70° C  |
| MK2302S-01LFT       | 230201LF  | Tape and Reel | 8-pin SOIC | 0 to +70° C  |
| MK2302S-01ILF       | 230201ILF | Tubes         | 8-pin SOIC | -40 to 85° C |
| MK2302S-01ILFT      | 230201ILF | Tape and Reel | 8-pin SOIC | -40 to 85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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