

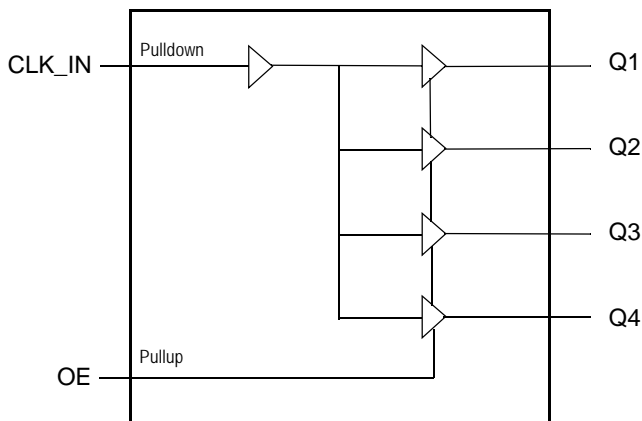
## General Description

The 830154I-08 is an LVC MOS, over-voltage tolerant clock fanout buffer targeted for clock generation in high-performance telecommunication, networking and computing applications. The device is optimized for low-skew clock distribution in low-voltage applications. The input over-voltage tolerance enables using this device in mixed-mode voltage applications. An output enable pin controls whether the outputs are in the active or high impedance state. Guaranteed output skew characteristics make the 830154I-08 ideal for those applications demanding well defined performance and repeatability. The 830154I-08 is packaged in a small 8-TSSOP and in an 8-SOIC package.

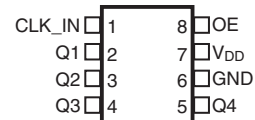
## Features

- Low-skew 1:4 fanout buffer
- Supports 3.3V, 2.5V, 1.8V and 1.5V power supplies
- LVC MOS input and output levels
- 3.6V Over-voltage tolerance at the clock and control inputs
- Supports clock frequencies up to 160MHz
- LVC MOS compatible control input for output disable
- Output disabled to a high-impedance state
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS 6 packages (8-TSSOP, 8-SOIC)

## Block Diagram



## Pin Assignments



### 830154AMI-08

8-SOIC, 150 mil

3.9mm x 4.9mm x 1.375mm package body

M-Package

Top View

### 830154AGI-08

8-TSSOP

4.4mm x 3.0mm x 0.925mm package body

G-Package

Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	CLK_IN	Input	Pulldown	Single-ended clock input. LVCMOS interface levels.
2	Q1	Output		Single-ended clock output. LVCMOS interface levels.
3	Q2	Output		Single-ended clock output. LVCMOS interface levels.
4	Q3	Output		Single-ended clock output. LVCMOS interface levels.
5	Q4	Output		Single-ended clock output. LVCMOS interface levels.
6	GND	Power		Power supply ground.
7	V <sub>DD</sub>	Power		Power supply pin.
8	OE	Input	Pullup	Output enable pin. See Table 3. LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> = 3.465V		14		pF
		V <sub>DD</sub> = 2.375V		13		pF
		V <sub>DD</sub> = 1.95V		13		pF
		V <sub>DD</sub> = 1.6V		12		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DD</sub> = 3.3V ± 5%		9		Ω
		V <sub>DD</sub> = 2.5V ± 5%		10		Ω
		V <sub>DD</sub> = 1.8V ± 0.15V		12		Ω
		V <sub>DD</sub> = 1.5 ± 0.1V		15		Ω

## Function Table

**Table 3. OE Configuration Table**

Input	Operation
OE	
0	Q[4:1] disabled (high-impedance)
1 (default)	Q[4:1] enabled

NOTE: OE is an asynchronous control.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	3.6V
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$ 8 Lead TSSOP 8 Lead SOIC	121.5°C/W (0 mps) 103°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{DDQ}$	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{DDQ}$	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

**Table 4C. Power Supply DC Characteristics,  $V_{DD} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		1.65	1.8	1.95	V
$I_{DDQ}$	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

**Table 4D. Power Supply DC Characteristics,  $V_{DD} = 1.5V \pm 0.1V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		1.4	1.5	1.6	V
$I_{DDQ}$	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

**Table 4E. LVCMOS DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$0.65 * V_{DD}$		3.6	V
$V_{IL}$	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
$I_{IH}$	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
		OE	$V_{DD} = V_{IN} = 3.465V$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK_IN	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu\text{A}$
		OE	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu\text{A}$
$V_{OH}$	Output High Voltage	Q[4:1]	$I_{OH} = -12\text{mA}$	2.6		V
$V_{OL}$	Output Low Voltage	Q[4:1]	$I_{OL} = 12\text{mA}$		0.5	V

**Table 4F. LVCMOS DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$0.65 * V_{DD}$		3.6	V
$V_{IL}$	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
$I_{IH}$	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 2.625V$		150	$\mu\text{A}$
		OE	$V_{DD} = V_{IN} = 2.625V$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK_IN	$V_{DD} = 2.625V, V_{IN} = 0V$	-5		$\mu\text{A}$
		OE	$V_{DD} = 2.625V, V_{IN} = 0V$	-150		$\mu\text{A}$
$V_{OH}$	Output High Voltage	Q[4:1]	$I_{OH} = -12\text{mA}$	1.8		V
$V_{OL}$	Output Low Voltage	Q[4:1]	$I_{OL} = 12\text{mA}$		0.5	V

**Table 4G. LVCMOS DC Characteristics,  $V_{DD} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$0.65 * V_{DD}$		3.6	V
$V_{IL}$	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
$I_{IH}$	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 1.95V$		150	$\mu\text{A}$
		OE			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK_IN	$V_{DD} = 1.95V, V_{IN} = 0V$	-5		$\mu\text{A}$
		OE	$V_{DD} = 1.95V, V_{IN} = 0V$	-150		$\mu\text{A}$
$V_{OH}$	Output High Voltage	Q[4:1]	$I_{OH} = -6\text{mA}$	$V_{DD} - 0.45$		V
$V_{OL}$	Output Low Voltage	Q[4:1]	$I_{OL} = 6\text{mA}$		0.45	V

**Table 4H. LVCMOS DC Characteristics,  $V_{DD} = 1.5V \pm 0.1V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$0.65 * V_{DD}$		3.6	V
$V_{IL}$	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
$I_{IH}$	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 1.6V$		150	$\mu A$
		OE	$V_{DD} = V_{IN} = 1.6V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK_IN	$V_{DD} = 1.6V, V_{IN} = 0V$	-5		$\mu A$
		OE	$V_{DD} = 1.6V, V_{IN} = 0V$	-150		$\mu A$
$V_{OH}$	Output High Voltage	Q[4:1]	$I_{OH} = -4mA$	$0.75 * V_{DD}$		V
$V_{OL}$	Output Low Voltage	Q[4:1]	$I_{OL} = 4mA$		$0.25 * V_{DD}$	V

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				160	MHz
$t_{PLH}$	Propagation Delay (low to high transition); NOTE 1		0.7		1.45	ns
$t_{PHL}$	Propagation Delay (high to low transition); NOTE 1		0.7		1.45	ns
$t_{PLZ}, t_{PHZ}$	Disable Time (active to high-impedance)				10	ns
$t_{PZL}, t_{PZH}$	Enable Time (high-impedance to disable)				10	ns
$tsk(o)$	Output Skew; NOTE 2, 3				250	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.094		ps
$t_R / t_F$	Output Rise/Fall Time	10% to 90%	0.35		1.2	ns
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized up to  $F_{OUT} \leq 150MHz$ .

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DD}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DD}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DD}/2$ .

**Table 5B. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				160	MHz
$t_{PLH}$	Propagation Delay (low to high transition); NOTE 1		0.8		1.7	ns
$t_{PHL}$	Propagation Delay (high to low transition); NOTE 1		0.8		1.7	ns
$t_{PLZ}$ , $t_{PHZ}$	Disable Time (active to high-impedance)				10	ns
$t_{PZL}$ , $t_{PZH}$	Enable Time (high-impedance to disable)				10	ns
$tsk(o)$	Output Skew; NOTE 2, 3				250	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.076		ps
$t_R / t_F$	Output Rise/Fall Time	10% to 90%	0.35		1.2	ns
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized up to  $F_{OUT} \leq 150MHz$ .

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DD}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DD}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DD}/2$ .

**Table 5C. AC Characteristics,  $V_{DD} = 1.8V \pm 0.15V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				160	MHz
$t_{PLH}$	Propagation Delay (low to high transition); NOTE 1		1.1		2.1	ns
$t_{PHL}$	Propagation Delay (high to low transition); NOTE 1		1.1		2.1	ns
$t_{PLZ}$ , $t_{PHZ}$	Disable Time (active to high-impedance)				10	ns
$t_{PZL}$ , $t_{PZH}$	Enable Time (high-impedance to disable)				10	ns
$tsk(o)$	Output Skew; NOTE 2, 3				250	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.193		ps
$t_R / t_F$	Output Rise/Fall Time	0.63V to 1.17V	0.12		0.6	ns
odc	Output Duty Cycle		47		53	%

For NOTES, see Table 5B above.

**Table 5D. AC Characteristics,  $V_{DD} = 1.5V \pm 0.1V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				160	MHz
$t_{PLH}$	Propagation Delay (low to high transition); NOTE 1		1.5		2.7	ns
$t_{PHL}$	Propagation Delay (high to low transition); NOTE 1		1.5		2.7	ns
$t_{PLZ}$ , $t_{PHZ}$	Disable Time (active to high-impedance)				10	ns
$t_{PZL}$ , $t_{PZH}$	Enable Time (high-impedance to disable)				10	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 3				250	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4				800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.266		ps
$t_R / t_F$	Output Rise/Fall Time	0.525V to 0.975V	0.12		0.6	ns
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized up to  $F_{OUT} \leq 150MHz$ .

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DD}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

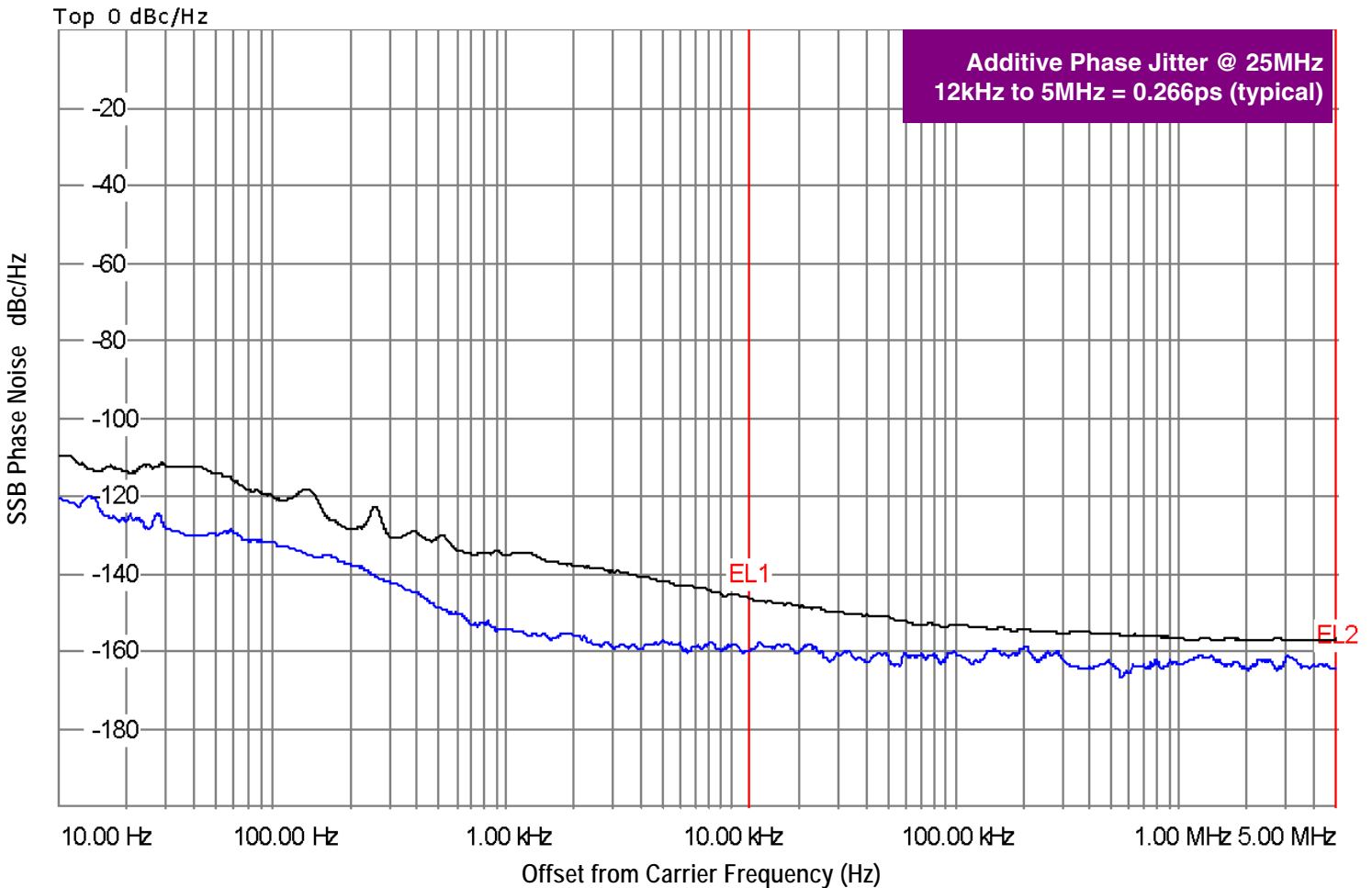
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DD}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DD}/2$ .

## Additive Phase Jitter (1.5V Output)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

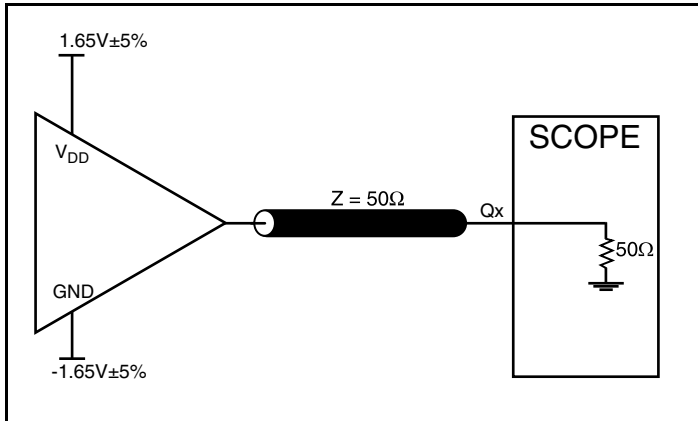


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

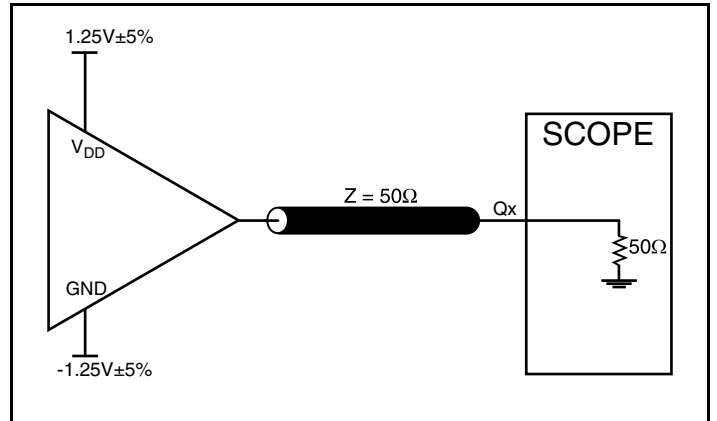
The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".



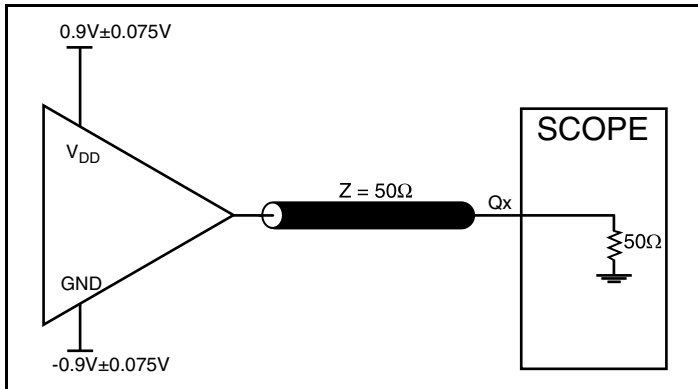
## Parameter Measurement Information



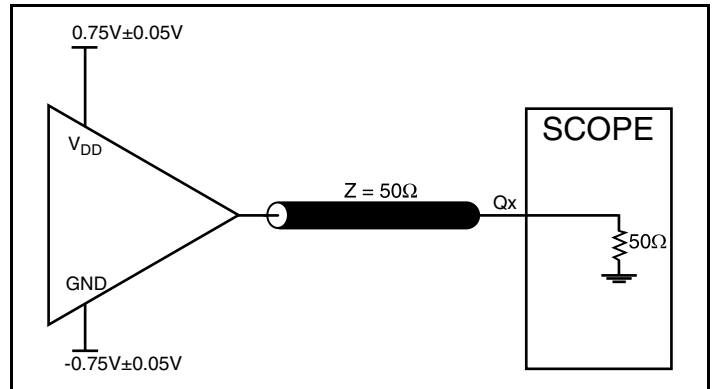
**3.3V Output Load AC Test Circuit**



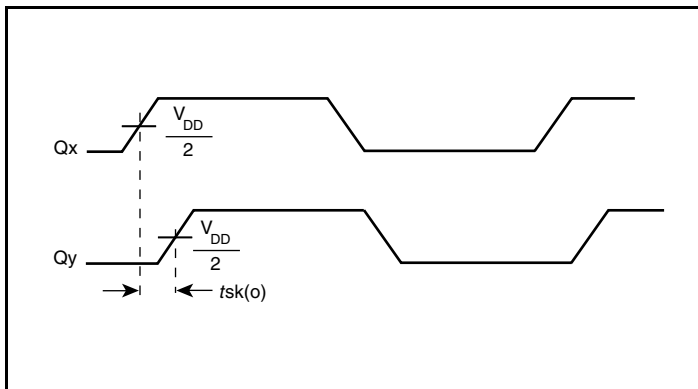
**2.5V Output Load AC Test Circuit**



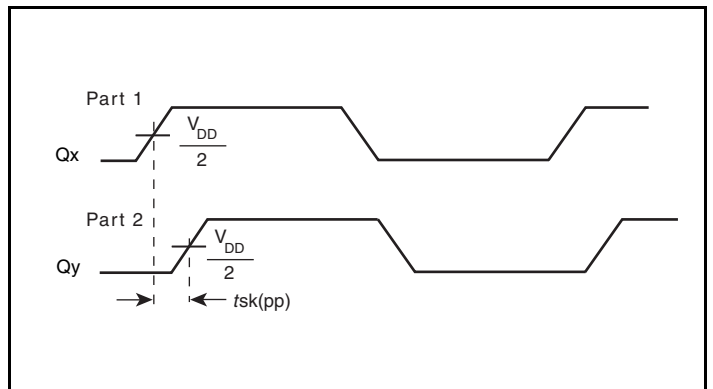
**1.8V Output Load AC Test Circuit**



**1.5V Output Load AC Test Circuit**

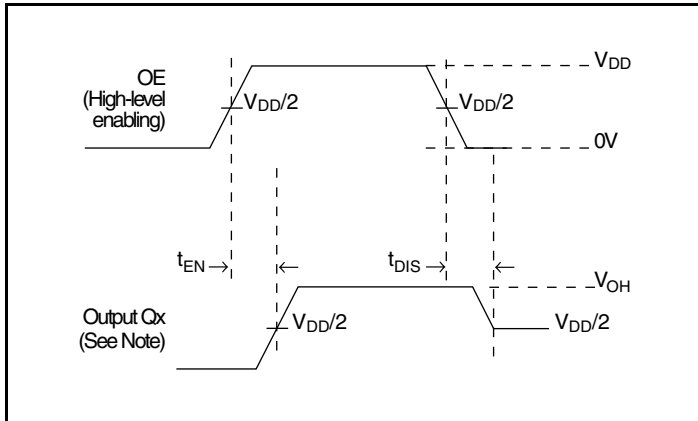


**Output Skew**

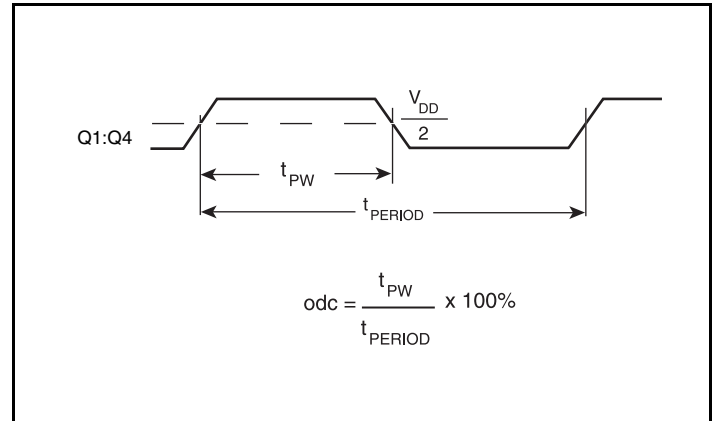


**Part-to-Part Skew**

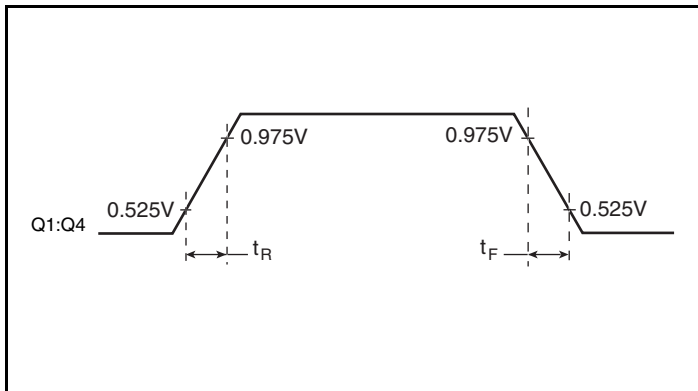
## Parameter Measurement Information, continued



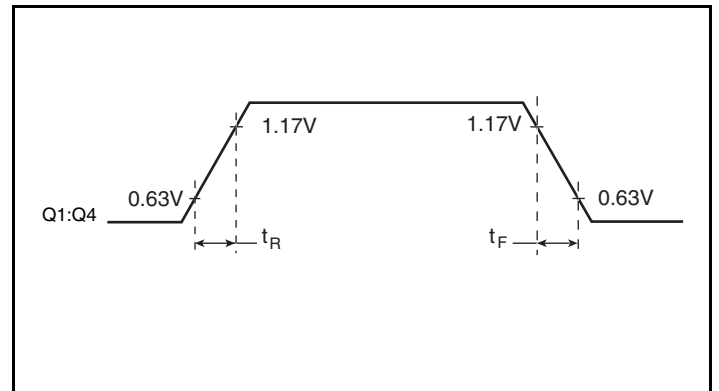
**Output Enable/Disable Time**



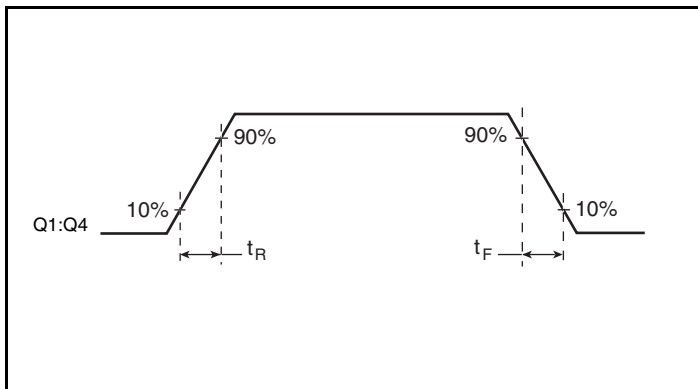
**Output Duty Cycle/Pulse Width/Period**



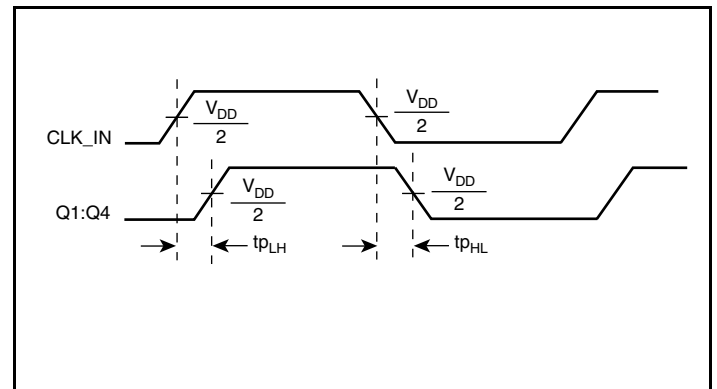
**1.5V Output Rise/Fall Time**



**1.8V Output Rise/Fall Time**



**2.5V and 3.3V Output Rise/Fall Time**



**Propagation Delay**

## Applications Information

### Recommendations for Unused Output Pins

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

## Power Considerations

This section provides information on power dissipation and junction temperature for the 830154I-08. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 830154I-08 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

$$\text{Power (core)}_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 1mA = \mathbf{3.465mW}$$

#### Total Static Power:

$$= \text{Power (core)}_{MAX} = \mathbf{3.465mW}$$

#### Dynamic Power Dissipation at $F_{OUT\_MAX}$ (160MHz)

$$\text{Total Power (160MHz)} = [(C_{PD} * N) * \text{Frequency} * (V_{DDO})^2] = [(14pF * 4) * 160MHz * (3.465V)^2] = \mathbf{107.6mW}$$

**N = number of outputs**

#### Total Power

$$\begin{aligned} &= \text{Static Power} + \text{Dynamic Power Dissipation} \\ &= 3.465mW + 107.6mW \\ &= \mathbf{111.065mW} \end{aligned}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 121.5°C/W per Table 6A below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.111W * 121.5^\circ\text{C/W} = 98.5^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6A. Thermal Resistance  $\theta_{JA}$  for 8 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	121.5°C/W	117.3°C/W	115.3°C/W

**Table 6B. Thermal Resistance  $\theta_{JA}$  for 8 Lead SOIC, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

## Reliability Information

**Table 7A.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead TSSOP**

$\theta_{JA}$ vs. Air Flow			
Meter per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	121.5°C/W	117.3°C/W	115.3°C/W

**Table 7B.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead SOIC**

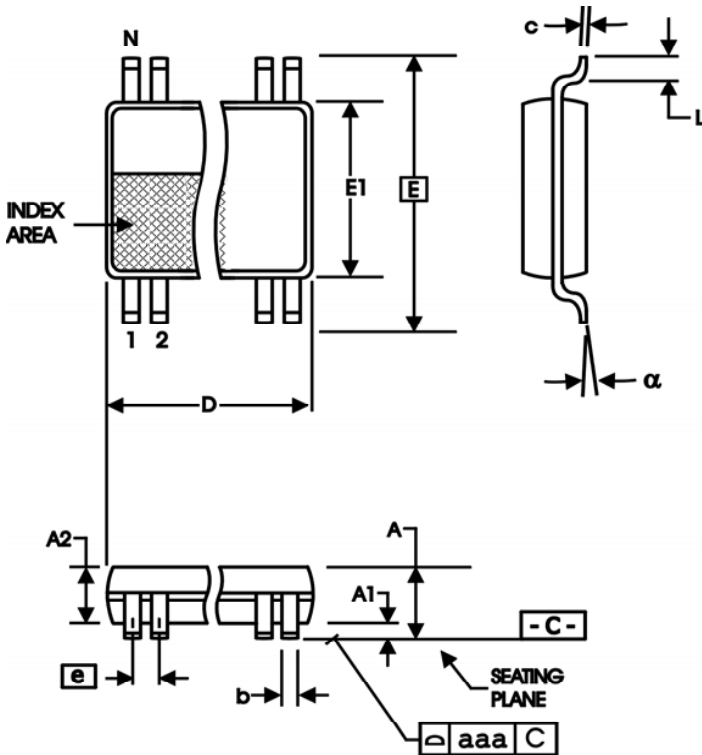
$\theta_{JA}$ vs. Air Flow			
Meter per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

## Transistor Count

The transistor count for 830154I-08 is: 191

## Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

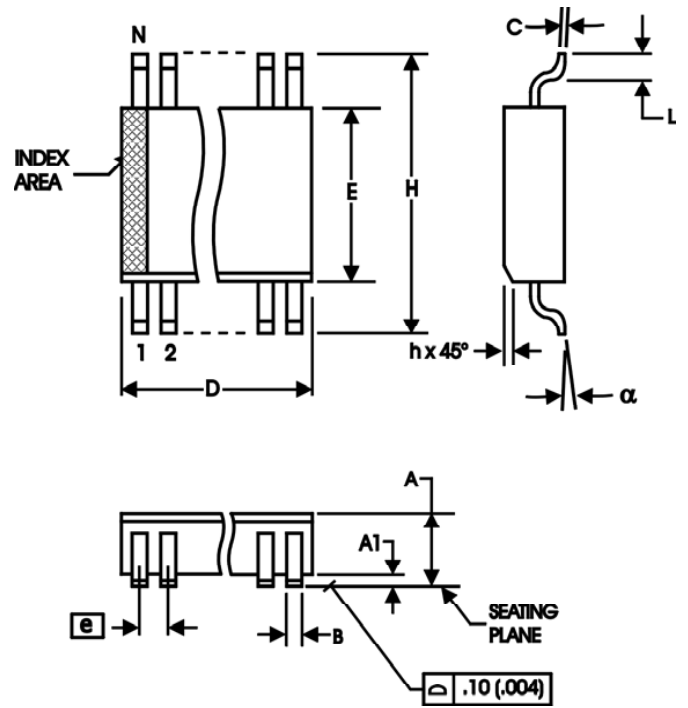


Table 8A. Package Dimensions for 8Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

## Ordering Information

**Table 9. Ordering Information**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
830154AGI-08LF	AI08L	Lead-Free, 8 Lead TSSOP	Tube	-40°C to 85°C
830154AGI-08LFT	AI08L	Lead-Free, 8 Lead TSSOP	Tape & Reel	-40°C to 85°C
830154AMI-08LF	154AI08L	Lead-Free, 8 Lead SOIC	Tube	-40°C to 85°C
830154AMI-08LFT	154AI08L	Lead-Free, 8 Lead SOIC	Tape & Reel	-40°C to 85°C

## Revision History

]

Revision Date	Description of Change
March 30, 2016	Removed ICS Chip from General Description. Removed ICS from part number where needed. Ordering Information - Removed quantity from tape and reel and deleted the LF note below the table. Updated data sheet header and footer.





Corporate Headquarters  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

Sales  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
[www.IDT.com/go/sales](http://www.IDT.com/go/sales)

Tech Support  
[www.idt.com/go/support](http://www.idt.com/go/support)

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners.

For datasheet type definitions and a glossary of common terms, visit [www.idt.com/go/glossary](http://www.idt.com/go/glossary).

Copyright ©2016 Integrated Device Technology, Inc. All rights reserved.