Low Voltage, Low Skew, PCI / PCI-X Clock Generator

8761

DATASHEET

General Description

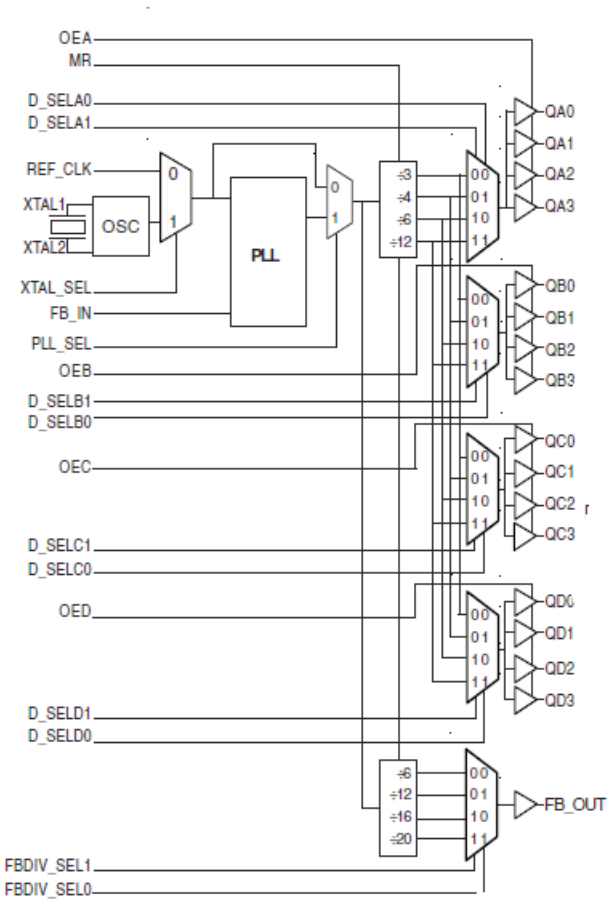
The 8761 is a low voltage, low skew PCI / PCI-X Clock Generator. The 8761 has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The 8761 has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with “zero delay”. Using a 20MHz or 25MHz crystal or a 33.333MHz or 66.666MHz reference frequency, the 8761 will generate output frequencies of 33.333MHz, 66.666MHz, 100MHz and 133.333MHz simultaneously.

The low impedance LVCMOS/LVTTL outputs of the 8761 are designed to drive 50Ω series or parallel terminated transmission lines.

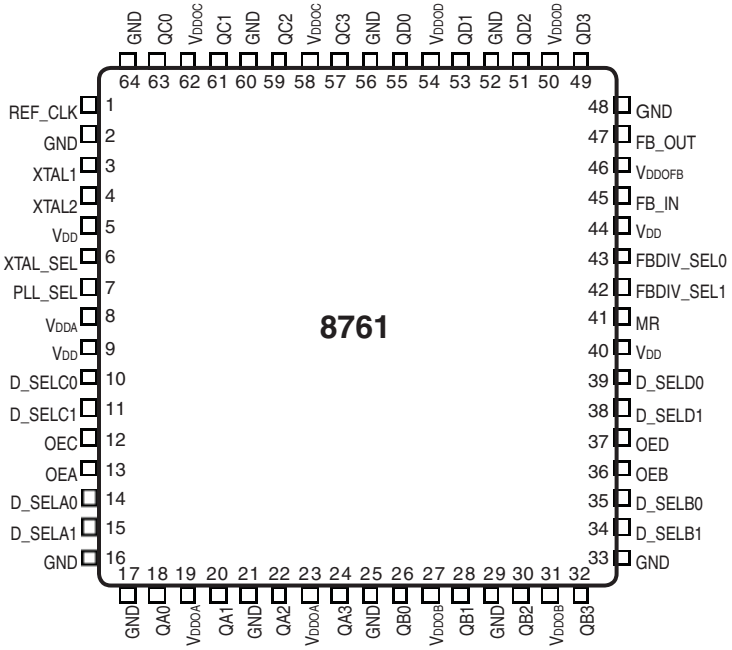
Features

- Fully integrated PLL
- Seventeen LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_CLK
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF_CLK input frequency: 83.33MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz simultaneously
- Separate feedback control for generating PCI / PCI-X frequencies from a 20MHz or 25MHz crystal or 33.333MHz or 66.666MHz reference frequency
- Cycle-to-cycle jitter: 70ps (maximum)
- Period jitter, RMS: 17ps (maximum)
- Output skew: 230ps (maximum)
- Bank skew: 40ps (maximum)
- Static phase offset: 0 ± 150ps (maximum)
- Full 3.3V or 3.3V core, 2.5V multiple output supply modes
- 0°C to 85°C ambient operating temperature
- Available in lead-free RoHS-compliant package

Block Diagram



Pin Assignment



64-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
2, 16, 17, 21, 25, 29, 33, 48, 52, 56, 60, 64	GND	Power		Power supply ground.
3, 4	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
5, 9, 40, 44	V_{DD}	Power		Core supply pins.
6	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS / LVTTL interface levels.
7	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin. See Applications Note for filtering.
10, 11	D_SELC0, D_SELC1	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3. LVCMOS / LVTTL interface levels.
12	OEC	Input	Pullup	Determines state of Bank C outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
13	OEA	Input	Pullup	Determines state of Bank A outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
14, 15	D_SELA0, D_SELA1	Input	Pulldown	Selects divider value for Bank A outputs as described in Table 3. LVCMOS / LVTTL interface levels.
18, 20, 22, 24	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
19, 23	V_{DDOA}	Power		Output supply pins for Bank A outputs.
26, 28, 30, 32	QB0, QB1, QB2, QB3	Output		Bank B clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
27, 31	V_{DDOB}	Power		Output supply pins for Bank B outputs.
34, 35	D_SELB1, D_SELB0	Input	Pulldown	Selects divider value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
36	OEB	Input	Pullup	Determines state of Bank B outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
37	OED	Input	Pullup	Determines state of Bank D outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
38, 39	D_SELD1, D_SELD0	Input	Pulldown	Selects divider value for Bank D outputs as described in Table 3. LVCMOS / LVTTL interface levels.
41	MR	Input	Pulldown	Active HIGH Master reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
42	FBDIV_SEL1	Input	Pulldown	Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
43	FBDIV_SEL0	Input	Pullup	Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
45	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with “zero delay”. LVCMOS / LVTTL interface levels.

Number	Name	Type		Description
46	V_{DDOFB}	Power		Output supply pin for FB_Out output.
47	FB_OUT	Output		Feedback output. Connect to FB_IN. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
49, 51, 53, 55	QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
50, 54	V_{DDOD}	Power		Output supply pins for Bank D outputs.
57, 59, 61, 63	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
58, 62	V_{DDOC}	Power		Output supply pins for Bank C outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor				51	kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51	kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA} = 3.465V; V_{DDOx} = 3.465V			9	pF
		V_{DD}, V_{DDA} = 3.465V; V_{DDOx} = 2.625V			11	pF
R_{OUT}	Output Impedance			15		Ω

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, V_{DDOFB}.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs					Outputs			
MR	OEA	OEB	OEC	OED	QA0:QA3	QB0:QB3	QC0:QC3	QD0:QD3
1	1	1	1	1	LOW	LOW	LOW	LOW
0	1	1	1	1	Active	Active	Active	Active
X	0	0	0	0	HiZ	HiZ	HiZ	HiZ

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
XTAL_SEL	PLL Input
0	REF_CLK
1	XTAL Oscillator

Table 3D. Control Function Table

Inputs					Outputs		
					PLL_SEL =1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency Range (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	41.6 - 83.33	x 2	83.33 - 166.67	41.6 - 83.33
0	0	0	1	20.83 - 41.67	x 4	83.33 - 166.67	20.83 - 41.67
0	0	1	0	15.62 - 31.25	x 5.33	83.33 - 166.67	15.62 - 31.25
0	0	1	1	12.5 - 25	x 6.67	83.33 - 166.67	12.5 - 25
0	1	0	0	41.6 - 83.33	x 1.5	62.4 - 125	41.6 - 83.33
0	1	0	1	20.83 - 41.67	x 3	62.4 - 125	20.83 - 41.67
0	1	1	0	15.62 - 31.25	x 4	62.4 - 125	15.62 - 31.25
0	1	1	1	12.5 - 25	x 5	62.4 - 125	12.5 - 25
1	0	0	0	41.6 - 83.33	x 1	41.6 - 83.33	41.6 - 83.33
1	0	0	1	20.83 - 41.67	x 2	41.6 - 83.33	20.83 - 41.67
1	0	1	0	15.62 - 31.25	x 2.67	41.6 - 83.33	15.62 - 31.25
1	0	1	1	12.5 - 25	x 3.33	41.6 - 83.33	12.5 - 25
1	1	0	0	41.6 - 83.33	÷ 2	20.8 - 41.67	41.6 - 83.33
1	1	0	1	20.83 - 41.67	÷ 1	20.8 - 41.67	20.83 - 41.67
1	1	1	0	15.62 - 31.25	x 1.33	20.8 - 41.67	15.62 - 31.25
1	1	1	1	12.5 - 25	x 1.67	20.8 - 41.67	12.5 - 25

NOTE: D_SELX1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1. D_SELX0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

Table 3E. Control Function Table (PCI Configuration)

Inputs					Outputs		
					PLL_SEL = 1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	66.67	x 2	133	66.67
0	0	0	1	33.33	x 4	133	33.33
0	0	1	0	25	x 5.33	133	25
0	0	1	1	20	x 6.67	133	20
0	1	0	0	66.67	x 1.5	100	66.67
0	1	0	1	33.33	x 3	100	33.33
0	1	1	0	25	x 4	100	25
0	1	1	1	20	x 5	100	20
1	0	0	0	66.67	x 1	66.67	66.67
1	0	0	1	33.33	x 2	66.67	33.33
1	0	1	0	25	x 2.67	66.67	25
1	0	1	1	20	x 3.33	66.67	20
1	1	0	0	66.67	÷ 2	33.33	66.67
1	1	0	1	33.33	÷ 1	33.33	33.33
1	1	1	0	25	x 1.33	33.33	25
1	1	1	1	20	x 1.67	33.33	20

NOTE: D_SELx1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1. D_SELx0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDOx} + 0.5V
Package Thermal Impedance, θ_{JA}	41.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				175	mA
I_{DDA}	Analog Supply Current				55	mA
I_{DDOx}	Output Supply Current; NOTE 2				25	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOFB}.
NOTE 2: I_{DDOx} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOFB}.

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDOx} = 2.5V \pm 5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				160	mA
I_{DDA}	Analog Supply Current				50	mA
I_{DDOx}	Output Supply Current; NOTE 2				210	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOFB}.
NOTE 2: I_{DDOx} denotes $_{IDDOA}$, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOFB}.

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1:D_SELD1, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		2		V_{DD} + 0.3	V
		REF_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1, D_SELD1, PLL_SEL		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL1	$V_{DD} = V_{IN} = 3.465V$			150	µA
		XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDOx} = 3.465V$	2.6			V
			$V_{DDOx} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDOx} = 3.465V$ or $2.625V$			0.5	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

NOTE 1: Outputs terminated with 50W to $V_{DDOx}/2$. See Parameter Measurement Information section, "Output Load Test Circuit" Diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance			7		pF
Drive Level				1	mW

TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		10		83.33	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1, 7	f = 50MHz	-150		150	ps
tsk(b)	Bank Skew; NOTE 2, 6				40	ps
tsk(o)	Output Skew; NOTE 3, 6				230	ps
tjit(cc)	Cycle-to-Cycle Jitter; 6	f = 50MHz; NOTE 4, 7			70	ps
		f = 25MHz XTAL, 133.3MHz out			190	ps
tjit(per)	Period Jitter, RMS; NOTE 4, 6, 7, 8				17	ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80%	300		800	ps
t_F	Output Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle; NOTE 5, 7		45		55	%

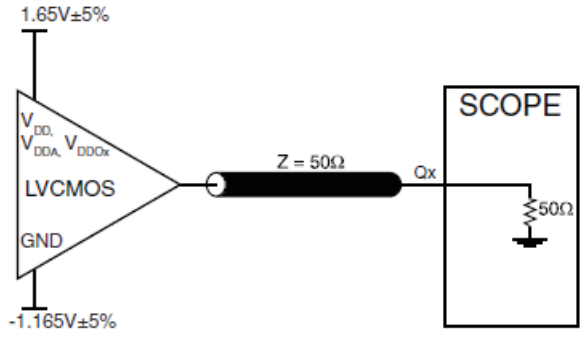
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured from $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Jitter performance using LVCMOS inputs.
NOTE 5: Measured using REF_CLK. For XTAL input, refer to Application Note.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: Tested with D_SELXX =10 (divide by 6); FBDIV_SEL = 00 (divide by 6).
NOTE 8: This parameter is defined as an RMS value.

TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDOx} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $85°C$

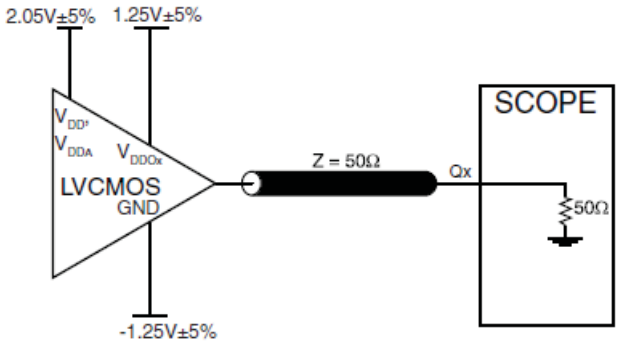
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1, 7	f = 50MHz	-350		20	ps
tsk(b)	Bank Skew; NOTE 2, 6				40	ps
tsk(o)	Output Skew; NOTE 3, 6				230	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 6	f = 50MHz; NOTE 4, 7			70	ps
		f = 25MHz XTAL, 133.3MHz out			190	ps
tjit(per)	Period Jitter, RMS; NOTE 4, 6, 7, 8				17	ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80%	300		800	ps
t_F	Output Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle; NOTE 5, 7		45		55	%

See notes in Table 7A above.

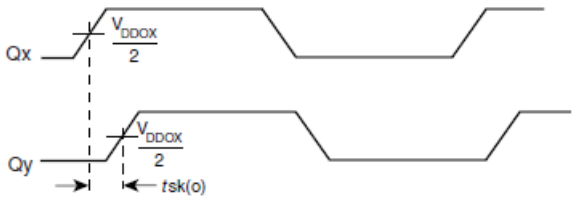
Parameter Measurement Information



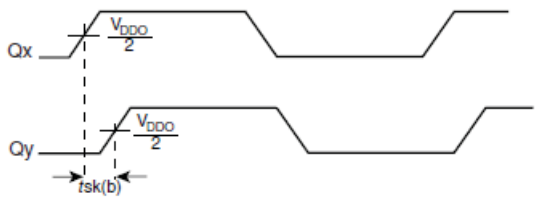
3.3V Output Load AC Test Circuit



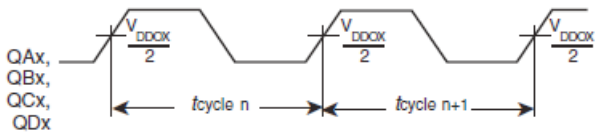
3.3V/2.5V Output Load AC Test Circuit



Output Skew



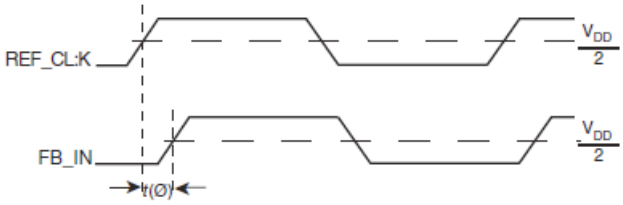
Bank Skew (Where X denotes outputs in the same Bank)



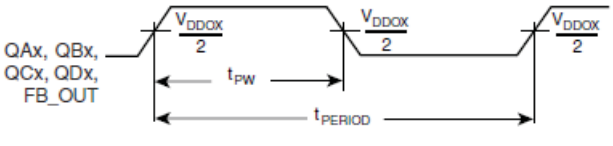
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

Cycle-to-Cycle Jitter

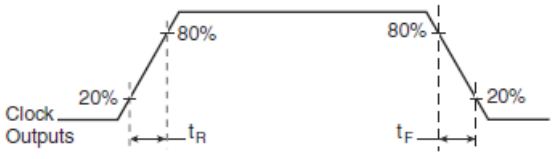


Static Phase Offset



$odc = \frac{t_{PW}}{t_{PERIOD}}$

Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 8761 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a ferrite bead along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

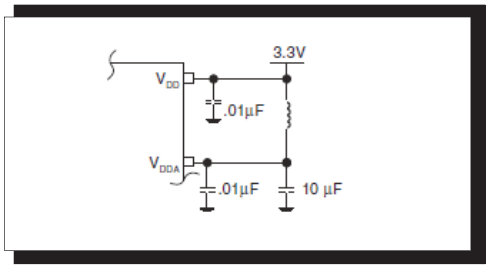


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 8761 crystal interface is shown in *Figure 2.* While layout the PC Board, it is recommended to provide C1 and C2 spare footprints for frequency fine tuning. For an 18pF parallel resonant crystal, the C1 and C2 are expected to be ~10pF and ~5pF respectively.

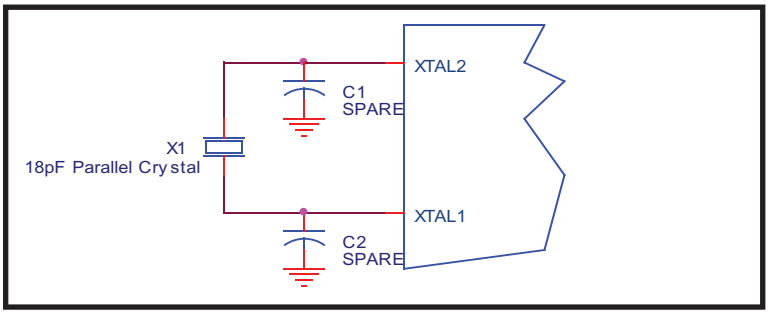


FIGURE 2. CRYSTAL INPUT INTERFACE

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Output:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Schematic Example

Figure 3 shows a schematic example of the 8761. In this example, the input is driven by an ICS LVHSTL driver. The decoupling capacitors should be physically located near the power pin. For 8761, the unused clock outputs can be left floating. The optional C1 and C2 are spare footprints for frequency fine tuning.

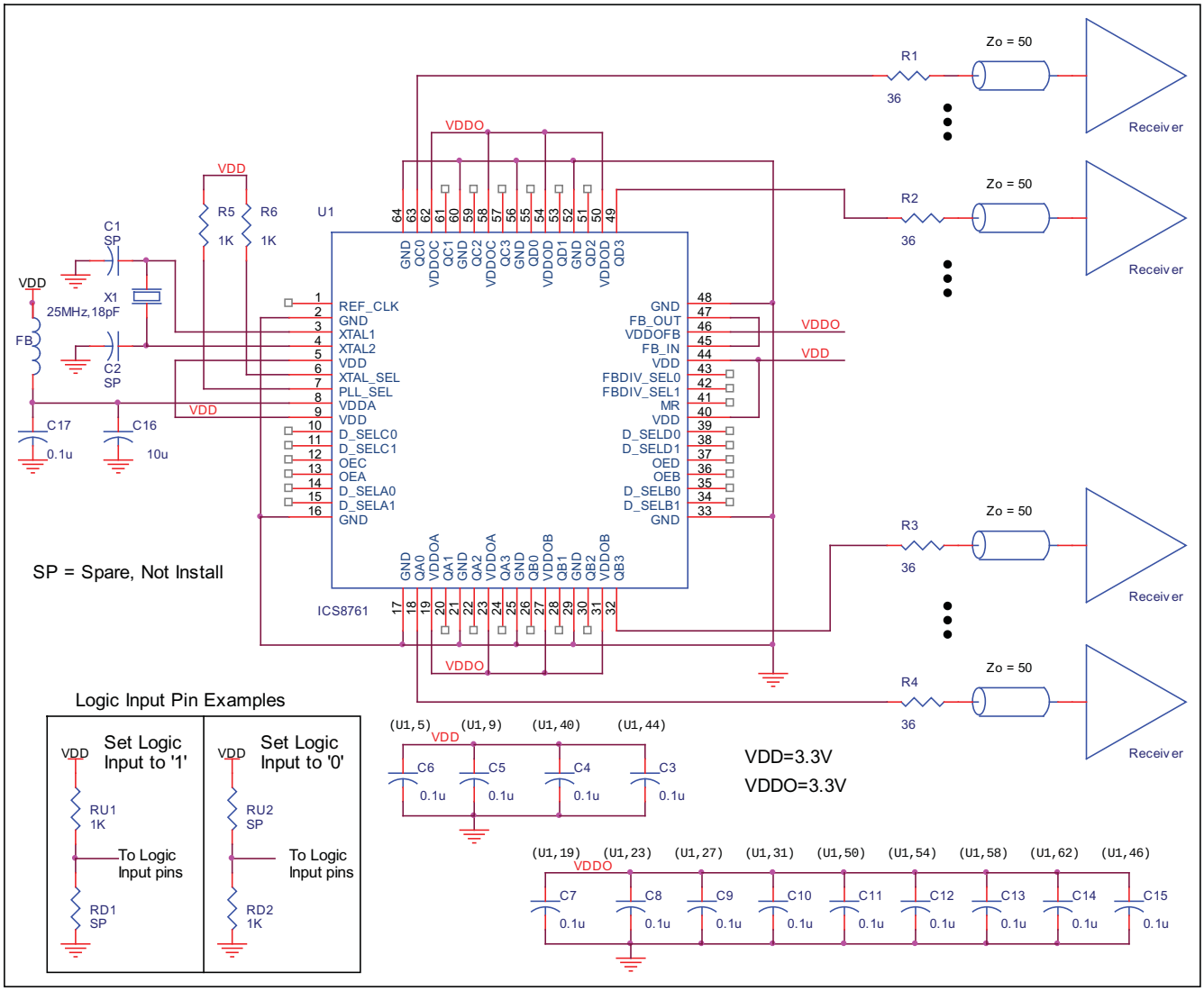


Figure 3. 8761 Clock Generator Schematic Example

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 64 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.8°C/W	48.5°C/W	43.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	41.1°C/W	35.8°C/W	33.6°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8761 is: 6040

Package Outline - Y Suffix for 64 Lead TSSOP

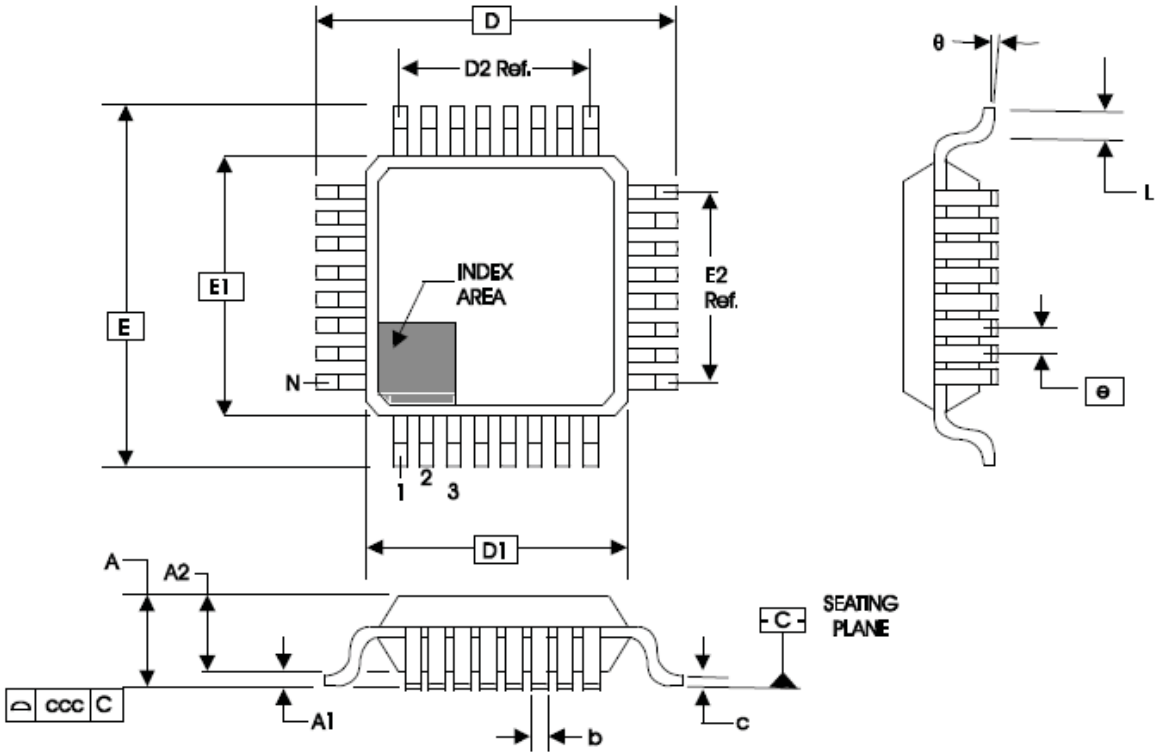


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCD		
	MINIMUM	NOMINAL	MAXIMUM
N		64	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	--	0.27
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.50 Ref.	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.50 Ref.	
e		0.50 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8761CYLF	ICS8761CYLF	64 Lead “Lead-Free” LQFP	tray	0°C to 85°C
8761CYLFT	ICS8761CYLF	64 Lead “Lead-Free” LQFP	tape & reel	0°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	2	Pin Description Table, revised Master Reset description.	8/15/02
A	T1 T4B, T4D	2 6, 8	Pin Description Table, pin 43 should be labeled at a PULLUP instead of a PULL-DOWN. LVCMOS DC Characteristics table -in the I_{IH} and I_{IL} rows, FBDIV_SEL0 was deleted from the “pulldown” row and was added to the “pullup” row.	11/05/02
B	T3D T5A, T5B	1 4 7, 9	Features section, changed max. output frequency from 200MHz to 183.3MHz, and max. REF_CLK input frequency from 100MHz to 91.6MHz. Control Function Table - revised Reference Frequency Range column and Frequency columns to reflect the output frequency change. AC Characteristics tables - changed Output Frequency from 200MHz max. to 183.3MHz max.	11/06/02
B	T1 T5A, T5B	2 7, 9 10 11	Pin Description Table, revised crystal description. AC Characteristics tables - changed Period Jitter measurement to Period Jitter, RMS and added NOTE 8. Added Crystal information. Added Schematic Example in the Application Information Section.	1/20/03
B	T1 T4A, T4C	2 5, 7 10 10	Pin Description Table - revised MR description. Power Supply Tables - changed V_{DD} parameter to read “Core Supply Voltage” from “Positive Supply Voltage”. Deleted Crystal Input Interface section. Updated Schematic Example diagram.	3/25/03
C	T3D T4A T5A & T5B	1 4 5 6 & 8	Updated Features to reflect T5A, 3.3V AC Characteristics (see below). Adjusted Ref. Frequency Range and Frequency columns. Changed I_{DD} max. from 150mA to 175mA, I_{DDA} max. from 50mA to 55mA, and I_{DDO} max. from 330mA to 25mA. Changed f_{MAX} from 183.3MHz max. to 166.67MHz max. Changed RMS tjit(per) from 20ps max. to 17ps max.	4/10/03
C		1 10 14	Features Section - added Lead-Free bullet. Added Crystal Section. Ordering Information Table - added Lead-Free/Annealed Part Number.	8/2/04
C		14	Ordering Information Table - added Lead-Free Part Number.	8/7/04
D	T2 T5 T10	3 6 9 10 11 14	Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical. Crystal Characteristics Table - added Drive Level. Power Supply Filtering Techniques - corrected last sentence in the paragraph to read “”Figure 1 illustrates how a ferrite bead along...”” from “”Figure 1 illustrates how a 10W resistor along...””. Corrected Power Supply Filtering diagram. Added Recommendations for Unused Input and Output Pins. Corrected Schematic Example diagram. Ordering Information Table - added Lead-Free note.	1/13/06
E	T10	 14 16	Updated datasheet’s header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/26/10
E	T10	14	Ordering Information - removed leaded devices PDN CQ-13-02	2/18/15

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