General Description

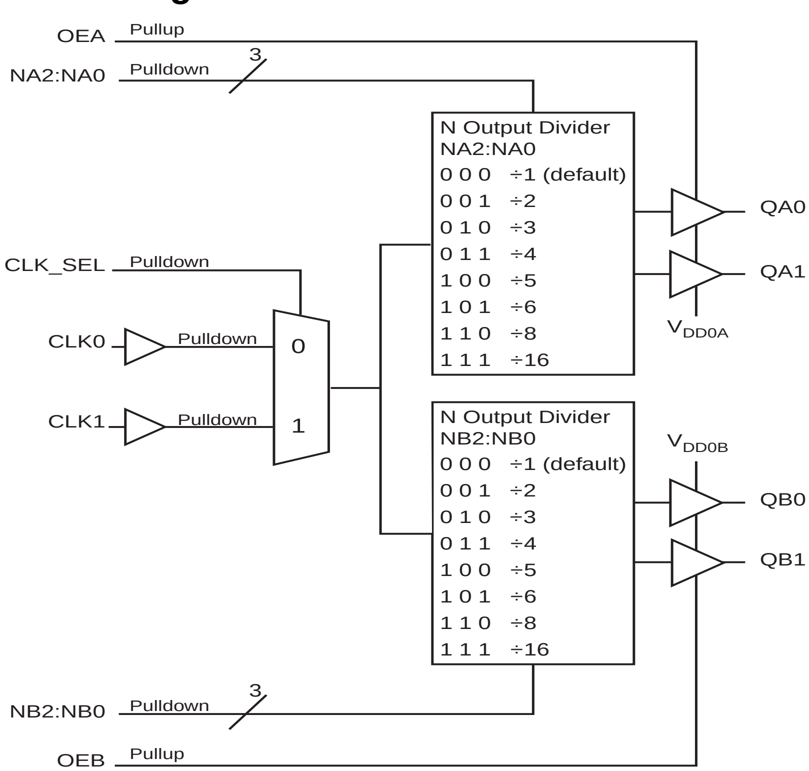
The ICS87004I-03 is a low skew, ÷1, ÷2 ÷3, ÷4 ÷5, ÷6 ÷8, ÷16 LVCMOS/LVTTL Fanout Buffer/Divider. The ICS87004I-03 has selectable clock inputs that accept single ended input levels. Output enable pin controls whether the output is in the active or high impedance state.

The ICS87004I-03 is characterized at 3.3V, 2.5V and mixed 3.3V,2.5V, 3.3V,1.8V, 2.5V,1.8V input/output supply operating modes.Guaranteed bank, output, and part-to-part skew characteristics make the ICS87004I-03 ideal for those applications demanding well defined performance and repeatability.

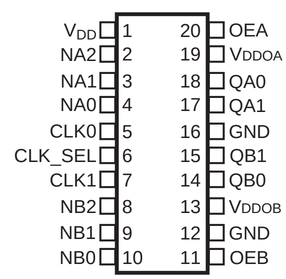
Features

- Two banks of two LVCMOS/LVTTL outputs
- Selectable LVCMOS/LVTTL clock inputs
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 40ps (typical)
- Bank skew: 20ps (typical)
- Part-to-part skew: 60ps (typical)
- Power supply modes:
  CORE / OUTPUT
  3.3V / 3.3V
  3.3V / 2.5V
  3.3V / 1.8V
  2.5V / 2.5V
  2.5V / 1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS87004I-03

20-Lead TSSOP
6.50mm x 4.40mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DD}	Power		Power supply pin.
2, 3, 4	NA2, NA1, NA0	Input	Pulldown	N divider select pins for Bank A outputs. LVCMOS / LVTTL interface levels.
5, 7	CLK0, CLK1	Input	Pulldown	Single-ended clock inputs. LVCMOS / LVTTL interface levels.
6	CLK_SEL	Input	Pulldown	Input clock selection. LVCMOS / LVTTL interface levels. See Table 6.
8, 9, 10	NB2, NB1, NB0	Input	Pulldown	N divider select pins for Bank B outputs. LVCMOS / LVTTL interface levels.
11	OEB	Input	Pullup	Output enable control input for Bank B outputs. LVCMOS / LVTTL interface levels. See Table 5.
12, 16	GND	Power		Power supply core ground.
13	V_{DDOB}	Power		Bank B output supply pin.
14, 15	QB0, QB1	Output		Single-ended Bank B clock outputs. LVCMOS / LVTTL interface levels.
17, 18	QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS / LVTTL interface levels.
19	V_{DDOA}	Power		Bank A output supply pin.
20	OEA	Input	Pullup	Output enable control input for Bank A outputs. LVCMOS / LVTTL interface levels. See Table 4.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DDOA} = V_{DDOB} = 3.465V$		10		pF
		$V_{DDOA} = V_{DDOB} = 2.625V$		10		pF
		$V_{DDOA} = V_{DDOB} = 1.95V$		10		pF
R_{OUT}	Output Impedance	$V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$		17		Ω
		$V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$		20		Ω
		$V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$		28		Ω

Function Table

Table 3. Programmable Output Divider Function Table

Inputs			N Divider Value	MAX Output Frequency (MHz)
NX2	NX1	NX0		
0	0	0	÷1 (default)	250
0	0	1	÷2	125
0	1	0	÷3	83.333
0	1	1	÷4	62.5
1	0	0	÷5	50
1	0	1	÷6	41.667
1	1	0	÷8	31.25
1	1	1	÷16	15.625

NOTE: Bank A and Bank B outputs are only synchronous if the same divider value is selected (NA2:0=NB2:0).

Table 4. OEA Function Table

OEA	Function
0	Bank A outputs are disabled in high-impedance state.
1 (default)	Bank A outputs are enabled

Table 5. OEB Function Table

OEB	Function
0	Bank B outputs are disabled in high-impedance state.
1 (default)	Bank B outputs are enabled

Table 6. Input Clock Selection

CLK_SEL	Input Clock
0 (default)	CLK0
1	CLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD}+ 0.5V
Outputs, V_O	-0.5V to V_{DDOX} + 0.5V
Package Thermal Impedance, θ_{JA}	91.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 7A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5% or 1.8V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
I_{DD}	Power Supply Current				55	mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No input clock or output loading			2	mA

Table 7B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5% or 1.8V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Current		2.375	2.5	2.625	V
			1.65	1.8	1.95	V
I_{DD}	Power Supply Current				55	mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No input clock or output loading			2	mA

Table 7C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, or 2.5V±5%, V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5% or 1.8V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	NA[2:0], NB[2:0], CLK[0:1], CLK_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OEA, OEB	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	NA[2:0], NB[2:0], CLK[0:1], CLK_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OEA, OEB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOA} = V_{DDOB} = 3.3V	2.6			V
			V_{DDOA} = V_{DDOB} = 2.5V	1.8			V
			V_{DDOA} = V_{DDOB} = 1.8V	1.25			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOA} = V_{DDOB} = 3.3Vor 2.5V			0.5	V
			V_{DDOA} = V_{DDOB} = 1.8V			0.4	V
I_{OZL}	Output Hi-Z Current Low			-5			µA
I_{OZH}	Output Hi-Z Current Low					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 8A. AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propgation Delay, NOTE 1	N≤ 2	3.8	4.8	5.8	ns
		N>2	4.0	5.5	7.0	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			50	300	ps
*t*sk(b)	Bank Skew: NOTE 3, 5			20	85	ps
t_R / t_F	OutputRise/Fall Time	20% to 80%	400	700	900	ps
odc	Output Duty Cycle	N=1	35		55	%
		N>1	40		60	%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at *ƒ*in ≤ 250MHz.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 8B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propgation Delay, NOTE 1	N≤ 2	4.0	5.0	6.0	
		N>2	4.5	6.0	7.5	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			60	550	ps
*t*sk(b)	Bank Skew: NOTE 3, 5			20	85	ps
t_R / t_F	OutputRise/Fall Time	20% to 80%	400	800	1200	ps
odc	Output Duty Cycle	N=1	35		55	%
		N>1	40		60	%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at *ƒ*in ≤ 250MHz.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 8C. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 1.8V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propgation Delay, NOTE 1	N≤ 2	4.0	5.5	7.0	ns
		N>2	4.8	6.3	7.8	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			60	600	ps
*t*sk(b)	Bank Skew: NOTE 3, 5			20	85	ps
t_R / t_F	OutputRise/Fall Time	20% to 80%	0.4	1	2.5	ns
odc	Output Duty Cycle	N=1	35		55	%
		N>1	40		60	%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at *f*in ≤ 250MHz
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 8D. AC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propgation Delay, NOTE 1	N≤ 2	4.0	5.0	6.0	ns
		N>2	4.5	6.0	7.5	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			50	350	ps
*t*sk(b)	Bank Skew: NOTE 3, 5			20	85	ps
t_R / t_F	OutputRise/Fall Time; NOTE 6	20% to 80%	400	900	1200	ps
odc	Output Duty Cycle	N=1	35		55	%
		N>1	40		60	%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

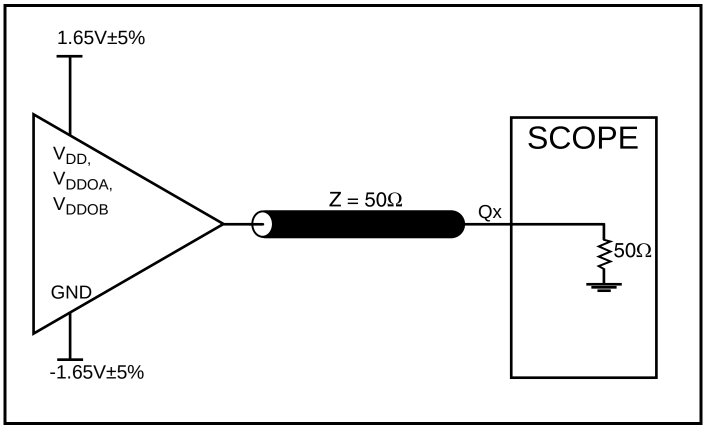
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at *f*in ≤ 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 8E. AC Characteristics, V_{DD} = 2.5V±5%, V_{DDOA} = V_{DDOB} = 1.8V±0.15V, T_A = -40°C to 85°C

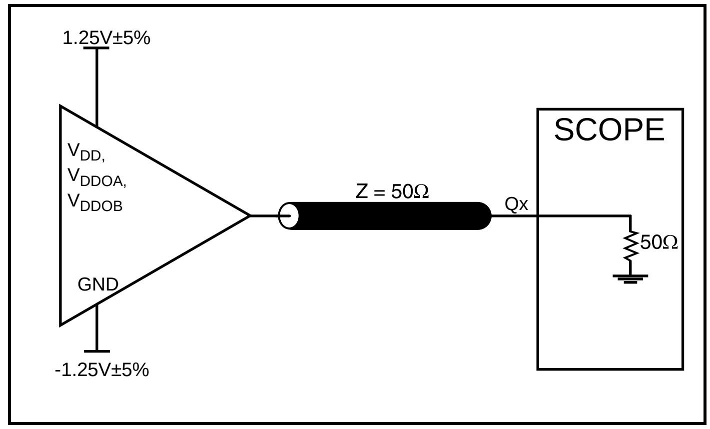
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propgation Delay, NOTE 1	N≤ 2	4.0	5.5	7.0	ns
		N>2	4.8	6.3	7.8	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			50	600	ps
*t*sk(b)	Bank Skew: NOTE 3, 5			20	85	ps
t_R / t_F	OutputRise/Fall Time; NOTE 6	20% to 80%	0.4	1.1	2.5	ns
odc	Output Duty Cycle	N=1	35		55	%
		N>1	40		60	
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at *ƒ*in ≤ 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

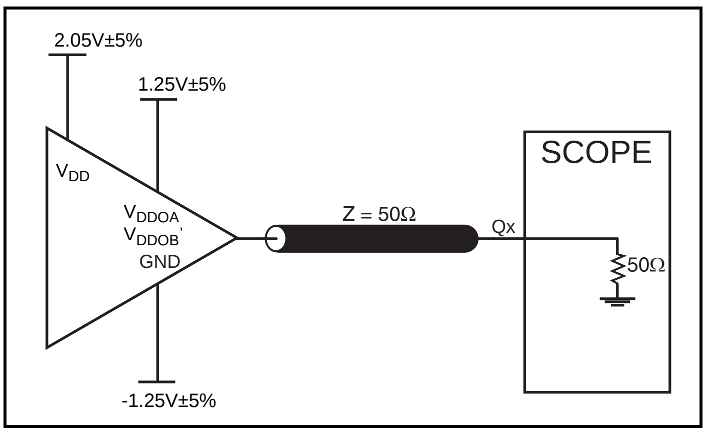
Parameter Measurement Information



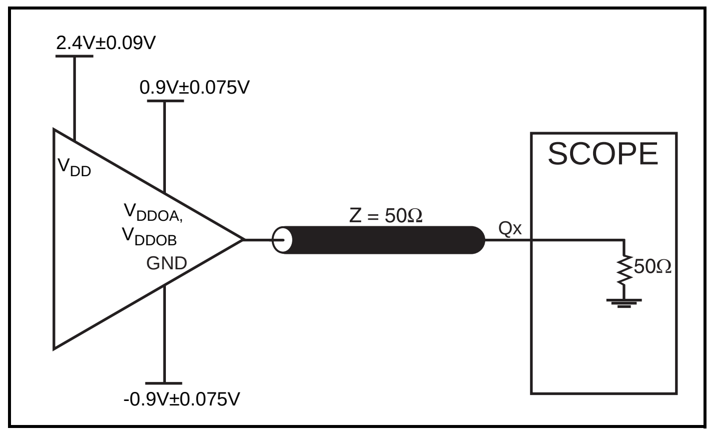
3.3V Core/3.3V Output Load AC Test Circuit



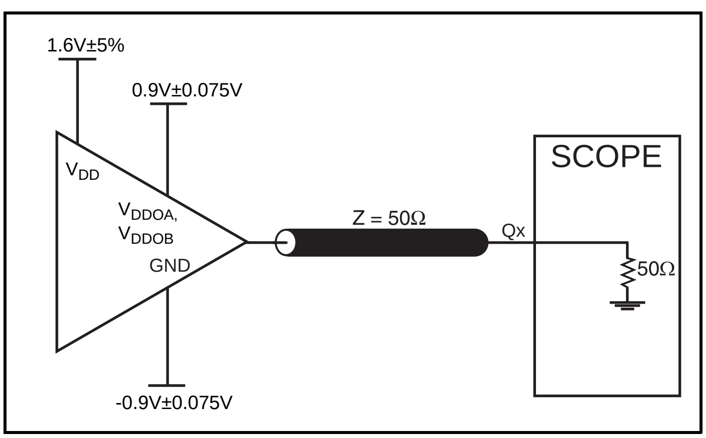
2.5V Core/2.5V Output Load AC Test Circuit



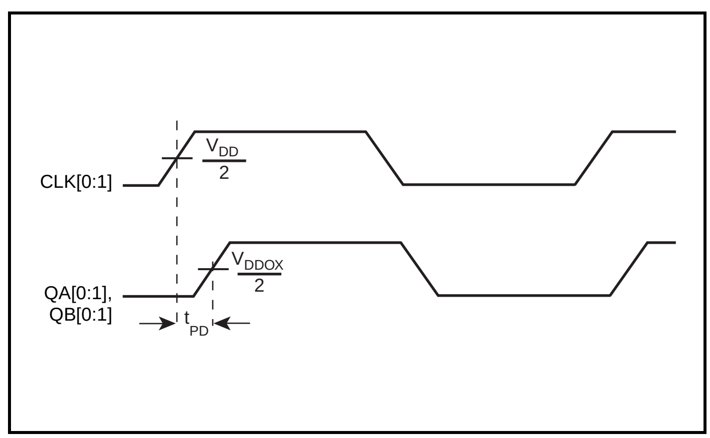
3.3V Core/2.5V Output Load AC Test Circuit



3.3V Core/1.8V Output Load AC Test Circuit

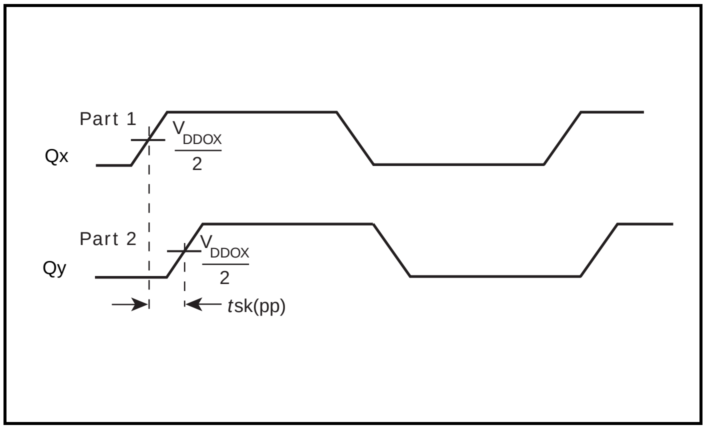


2.5V Core/1.8V Output Load AC Test Circuit

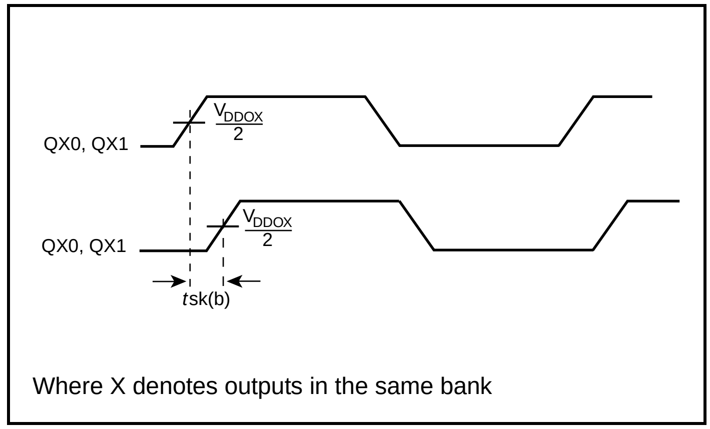


Propagation Delay

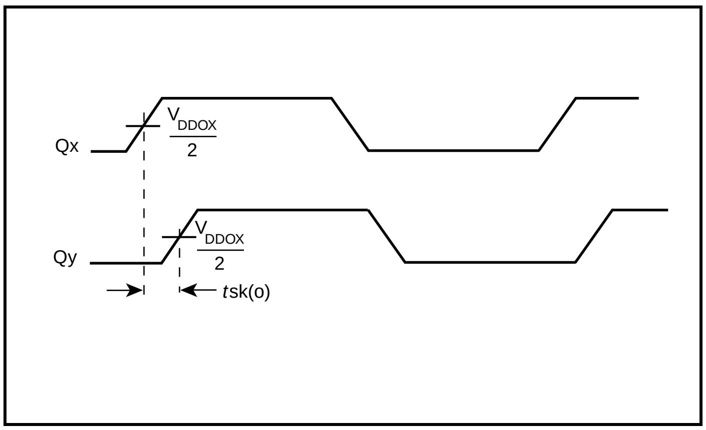
Parameter Measurement Information, continued



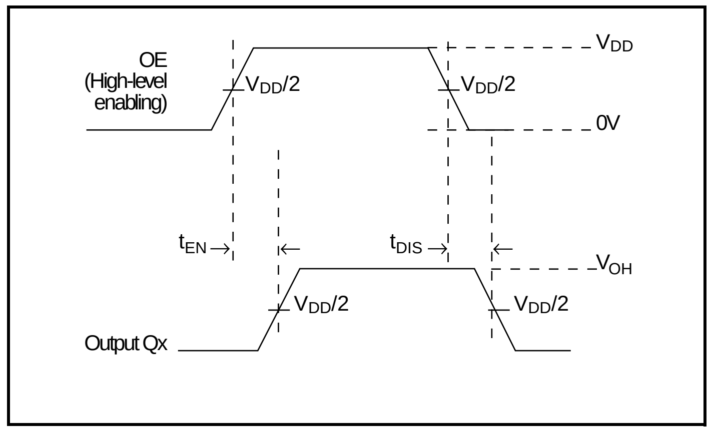
Part-to-Part Skew



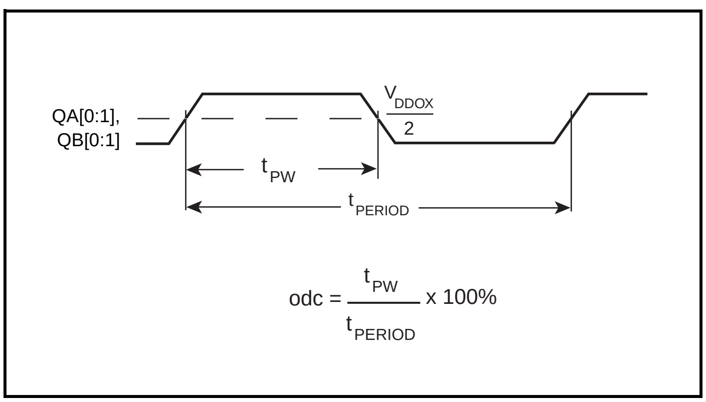
Bank Skew



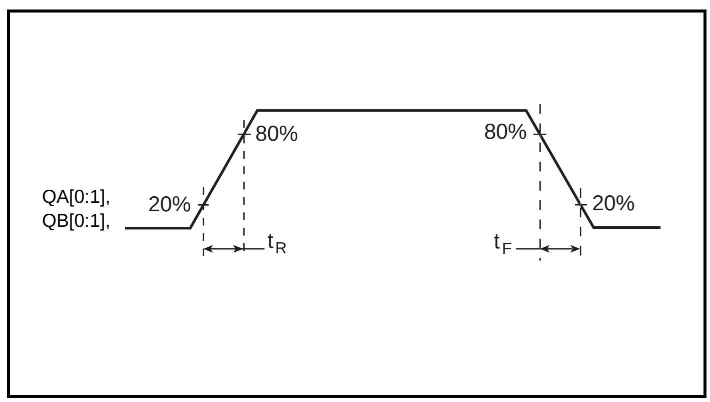
Output Skew



Output Enable/Disable



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating We recommend that there is no trace attached.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS87004I-03.

1. Power Dissipation.

The total power dissipation for the ICS87004I-03 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDOX})$ = 3.465V *(55mA + 2mA) = **197.51mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})]$ = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.7mW per output**
- Total Power (R_{OUT}) = 10.7mW * 4 = **42.6mW**

Dynamic Power Dissipation at 250MHz

Power (250MHz) = $(C_{PD} + C_L)$ * Frequency * $(V_{DD})^2$ =15pF * 250MHz * $(3.465V)^2$ = **45.02mW per output**

Total Power (250MHz) = 45.02mW * 4 = **180.09mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (250MHz)
  = 197.51mW + 42.6mW + 180.90mW
  = 420.22mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.420W *91.1°C/W = 123.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Reliability Information

Table 10. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Transistor Count

The transistor count for ICS87004I-03 is: 2769

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

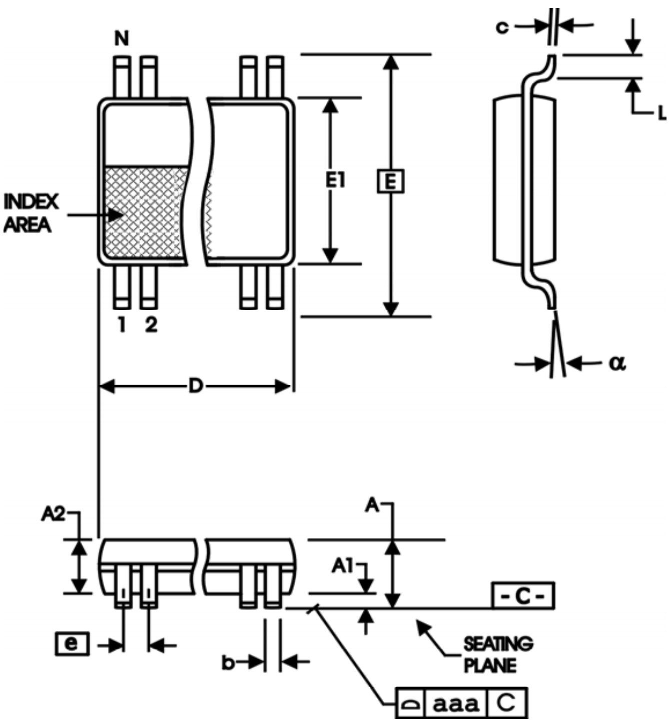


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87004BGI-03LF	ICS7004BI03L	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
87004BGI-03LFT	ICS7004BI03L	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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