

### Description

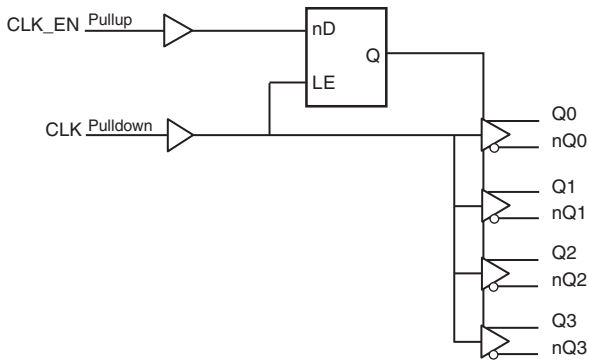
The 8545-01 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS) the 8545-01 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The 8545-01 accepts a LVCMOS/LVTTL input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the 8545-01 ideal for those applications demanding well defined performance and repeatability.

### Features

- Four differential LVDS output pairs
- Two LVCMOS/LVTTL clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency: 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 3.6ns (maximum)
- Full 3.3Vsupply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment

GND	1	20	Q0
CLK_EN	2	19	nQ0
nc	3	18	VDD
CLK	4	17	Q1
nc	5	16	nQ1
nc	6	15	Q2
nc	7	14	nQ2
nc	8	13	GND
GND	9	12	Q3
VDD	10	11	nQ3

**8545-01**  
**20-Lead TSSOP**  
**6.5mm x 4.4mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 9, 13	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, $\bar{Q}$ outputs are forced high. LVCMOS / LVTTTL interface levels.
3, 5, 6, 7, 8	nc	Unused		No connect.
4	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTTL interface levels.
10, 18	V <sub>DD</sub>	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

**Table 3. Clock Input Function Table**

Input	Outputs	
	Q0:Q3	nQ0:nQ3
0	LOW	HIGH
1	HIGH	LOW

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	91.1°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				50	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		CLK_EN	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		CLK_EN	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**Table 4C. LVDS DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		200	280	360	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				40	mV
$V_{OS}$	Offset Voltage		1.125	1.25	1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			5	25	mV
$I_{OZ}$	High Impedance Leakage		-10	$\pm 1$	+10	$\mu A$
$I_{OFF}$	Power Off Leakage		-20	$\pm 1$	+20	$\mu A$
$I_{OSD}$	Differential Output Short Circuit Current			-3.5	-5	mA
$I_{OS}$	Output Short Circuit Current			-3.5	-5	mA
$V_{OH}$	Output Voltage High			1.34	1.6	V
$V_{OL}$	Output Voltage Low		0.9	1.06		V

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				650	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.4		3.6	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				500	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	150		500	ps
odc	Output Duty Cycle	$f \leq 266MHz$	45		55	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to the differential output crossing point.

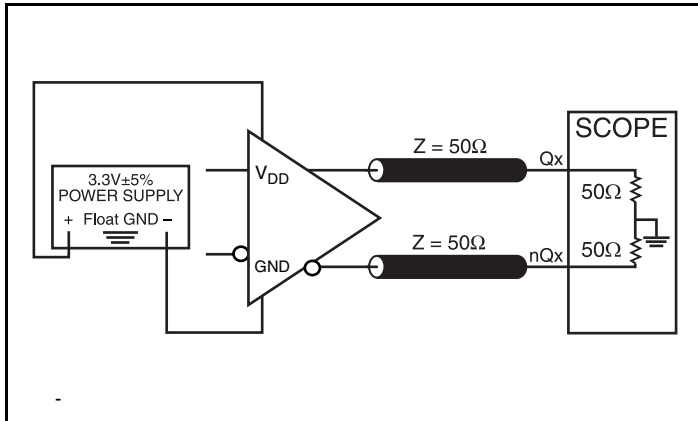
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DD}/2$  of the input to the differential output crossing point.

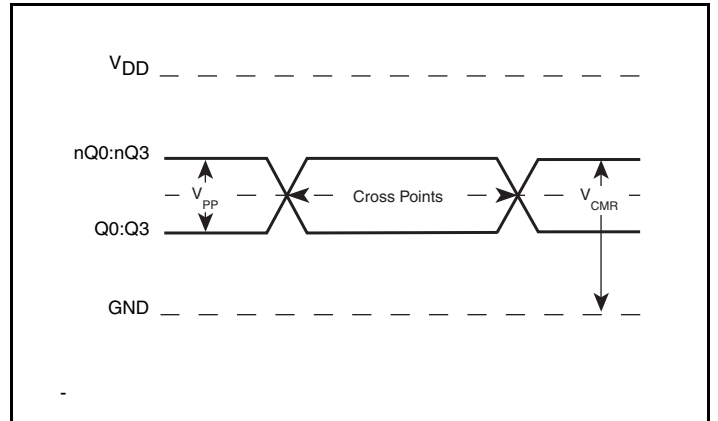
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

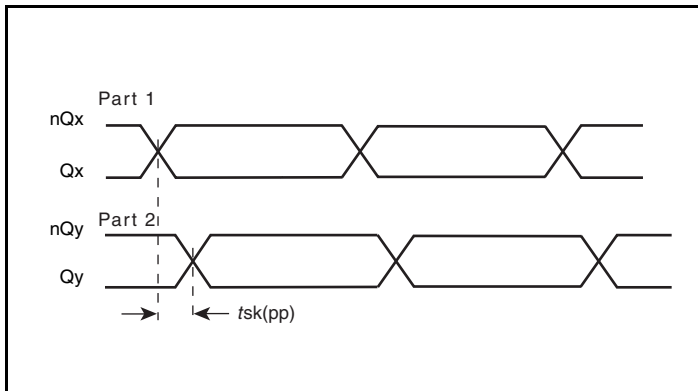
## Parameter Measurement Information



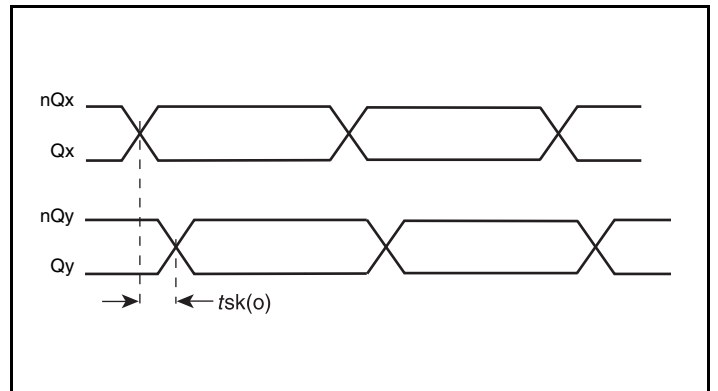
**3.3V LVDS Output Load AC Test Circuit**



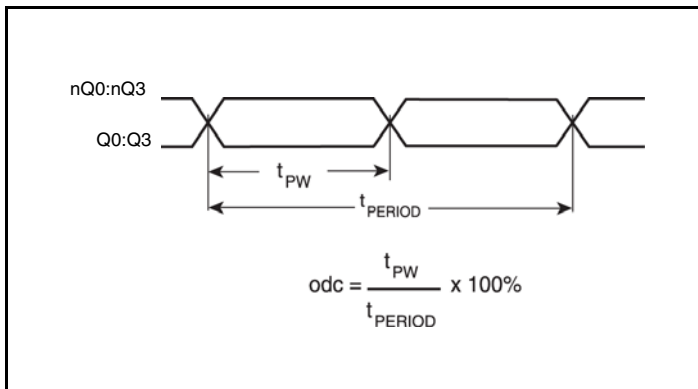
**Differential Output Level**



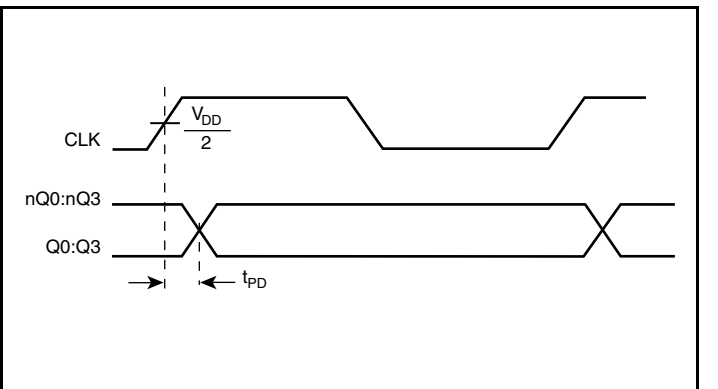
**Part-to-Part Skew**



**Output Skew**

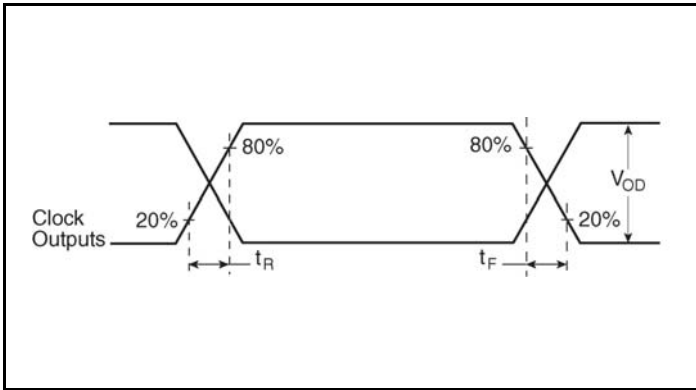


**Output Duty Cycle/Pulse Width/Period**

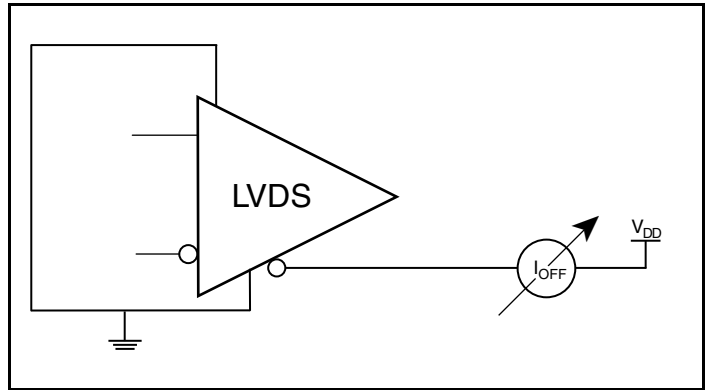


**Propagation Delay**

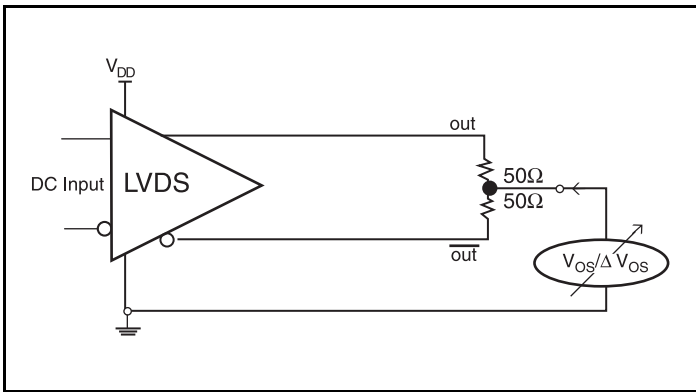
Parameter Measurement Information, continued



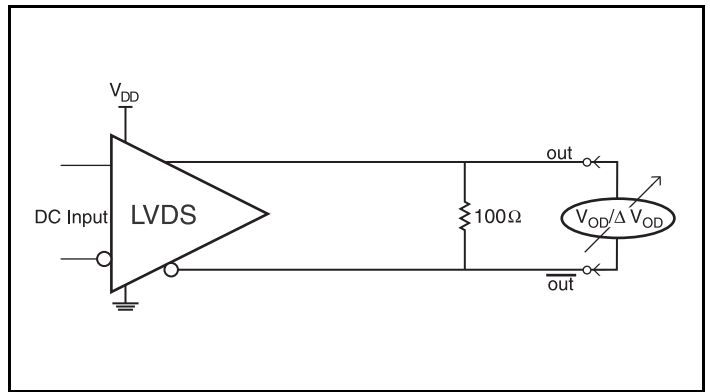
Output Rise/Fall Time



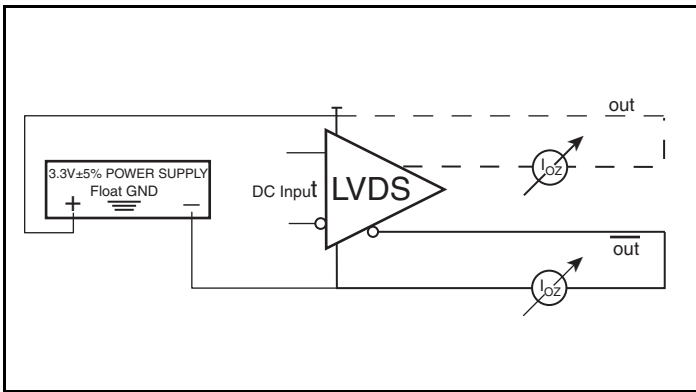
Power Off Leakage Setup



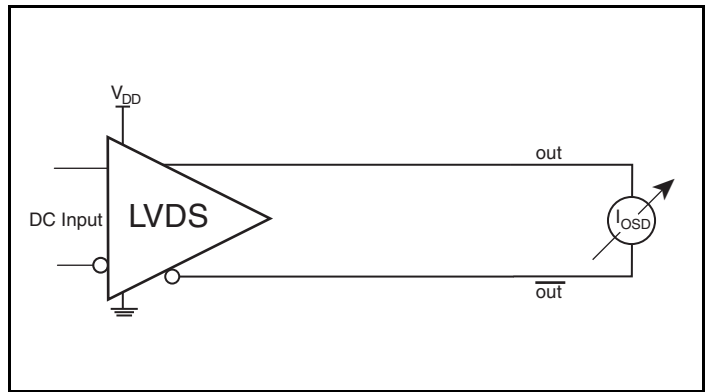
Offset Voltage Setup



Differential Output Voltage Setup

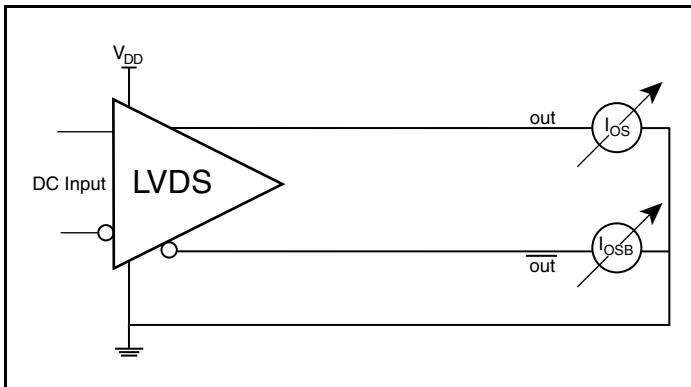


High Impedance Leakage Current Setup



Differential Output Short Circuit Setup

## Parameter Measurement Information, continued



**Output Short Circuit Current Setup**

## Application Information

### Recommendations for Unused Output Pins

#### Outputs:

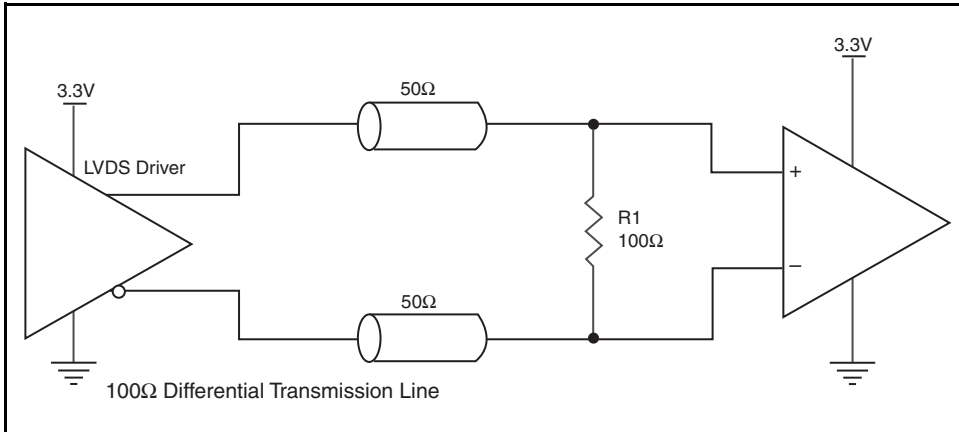
##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

### 3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 1. In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



**Figure 1. Typical LVDS Driver Termination**



## Power Considerations

This section provides information on power dissipation and junction temperature for the 8545-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8545-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 50mA = 173.25mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.173\text{W} * 91.1^\circ\text{C/W} = 85.7^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters Per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ by Velocity			
Meters Per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

## Transistor Count

The transistor count for 8545-01 is: 644

## Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

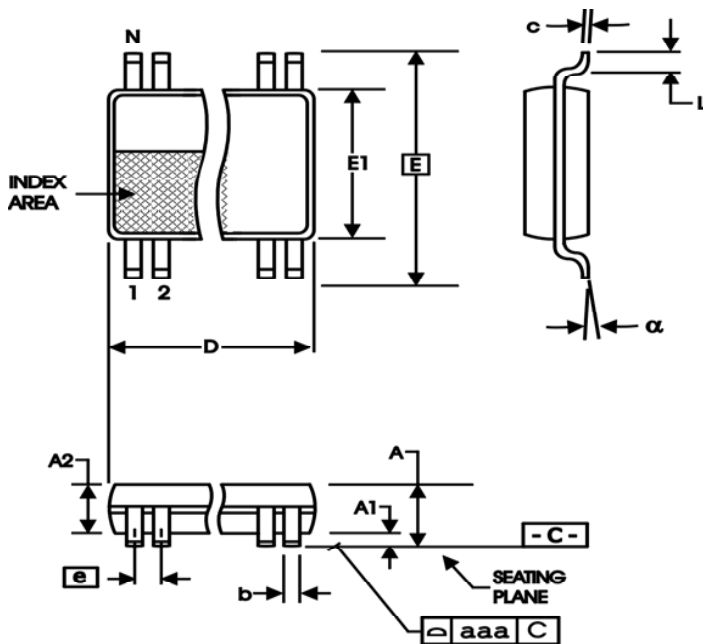


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8545AG-01LF	ICS8545AG01L	"Lead-Free" 20 Lead TSSOP	Tube	0°C to 70°C
8545AG-01LFT	ICS8545AG01L	"Lead-Free" 20 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	11	Ordering Information - removed leaded devices. Updated data sheet format.	7/10/15



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