FemtoClock® Crystal-to-LVDS Frequency Synthesizer

844008I-01

DATASHEET

General Description

The 844008I-01 is an 8 output LVDS Synthesizer optimized to generate GbE/10GbE reference clock frequencies. Using a 25MHz parallel resonant crystal, the following frequencies can be generated based on the F_SEL pin: 125MHz or 156.25MHz. The 844008I-01 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting GbE/10GbE jitter requirements. The 844008I-01 is packaged in a 32-pin TQFP or 32 VFQFN packages.

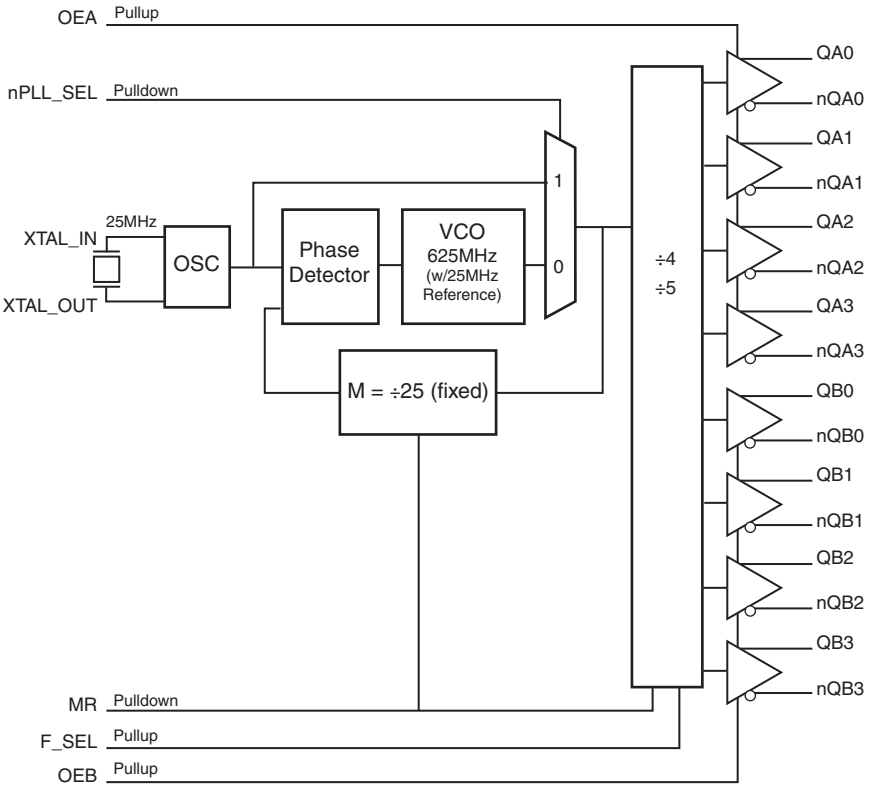
Features

- Eight LVDS outputs
- Crystal oscillator interface
- Supports the following output frequencies: 125MHz or 156.25MHz
- VCO: 625MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.38ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

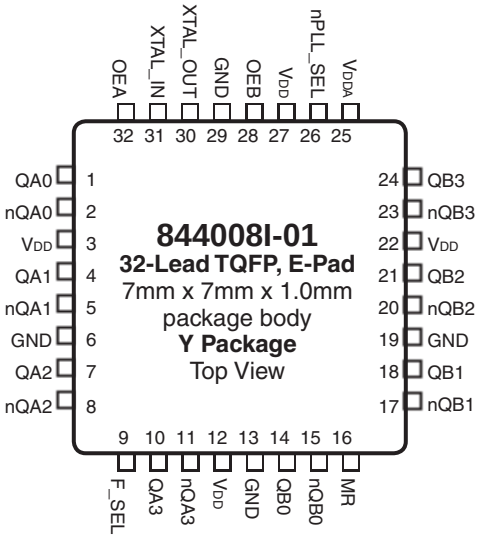
Frequency Select Function Table

Input				
Input Frequency (MHz)	F_SEL	M Divider Value	N Divider Value	Output Frequency (MHz)
25MHz	0	25	4	156.25
25MHz	1	25	5	125 (default)

Block Diagram



Pin Assignment



844008I-01
32-Lead TQFP, E-Pad
7mm x 7mm x 1.0mm
package body
Y Package
Top View

844008I-01
32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
3, 12, 22, 27	V_{DD}	Power		Core supply pins.
4, 5	QA1, nQA1	Ouput		Differential output pair. LVDS interface levels.
6, 13, 19, 29	GND	Power		Power supply ground.
7, 8	QA2, nQA2	Output		Differential output pair. LVDS interface levels.
9	F_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
10, 11	QA3, nQA3	Output		Differential output pair. LVDS interface levels.
14, 15	QB0, nQB0	Output		Differential output pair. LVDS interface levels.
16	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs to go low and the inverted output to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
17, 18	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
20, 21	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
23, 24	nQB3, QB3	Output		Differential output pair. LVDS interface levels.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_SEL	Input	Pulldown	Selects between the PLL and XTAL as input to the dividers. When LOW, selects PLL (PLL enabled). When HIGH, selects the XTAL (PLL bypassed). LVCMOS/LVTTL interface levels.
28	OEB	Input	Pullup	Output enable for QB[0:3]/nQB[0:3] outputs. See Table 3B. LVCMOS/LVTTL interface levels.
30, 31	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
32	OEA	Input	Pullup	Output enable for QA[0:3]/nQA[0:3] outputs. See Table 3A. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3A. OEA Function Table

Input	Outputs
OEA	**QA[0:3], nQA[0:3]**
0	High Impedance state
1	Normal operation

Table 3B. OEB Function Table

Input	Outputs
OEB	**QB[0:3], nQB[0:3]**
0	High Impedance state
1	Normal operation

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	
32 TQFP, E-Pad	32.2°C/W (0 mps)
32 VFQFN	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
I_{DD}	Power Supply Current				275	mA
I_{DDA}	Analog Supply Current				20	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	MR, nPLL_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
		OEA, OEB, F_SEL	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR, nPLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OEA, OEB, F_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		325		550	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2	1.3	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				5	pF

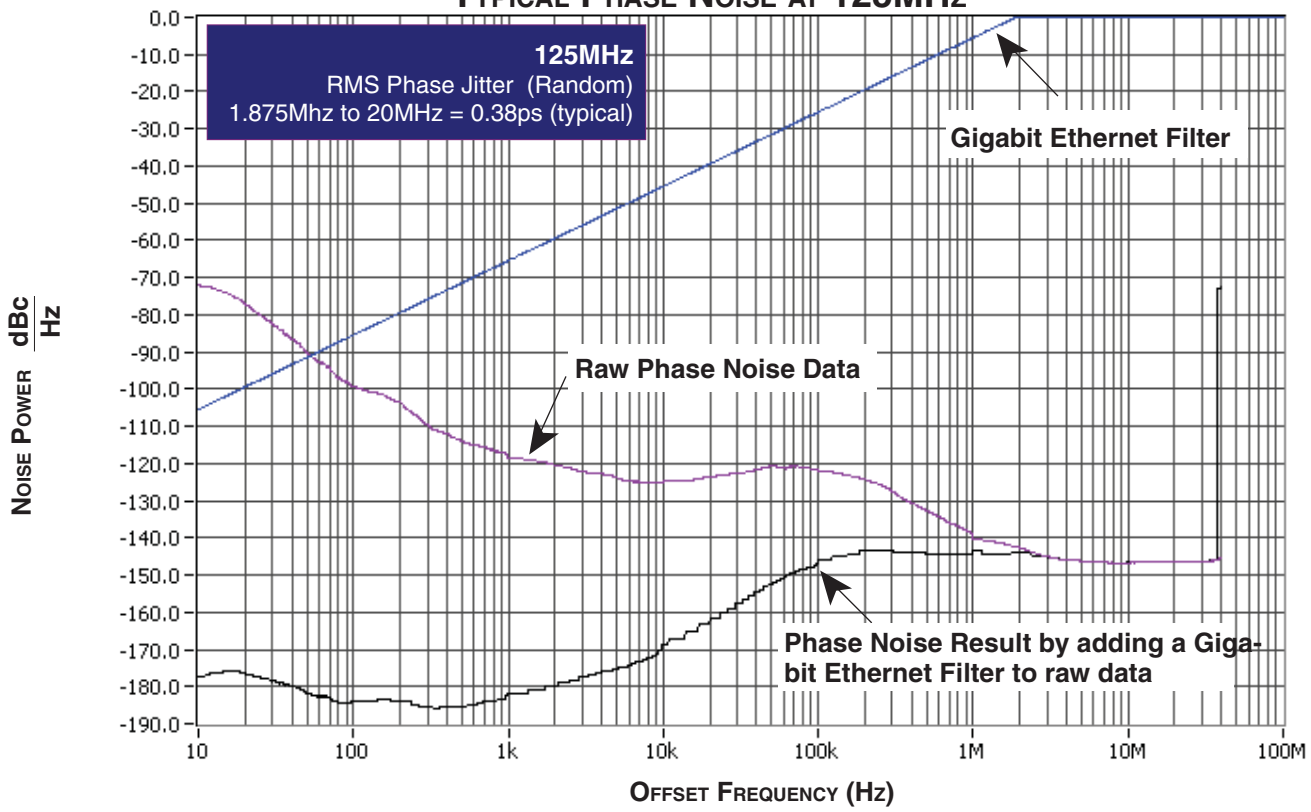
NOTE: Characterized using an18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = -40°C TO 85°C

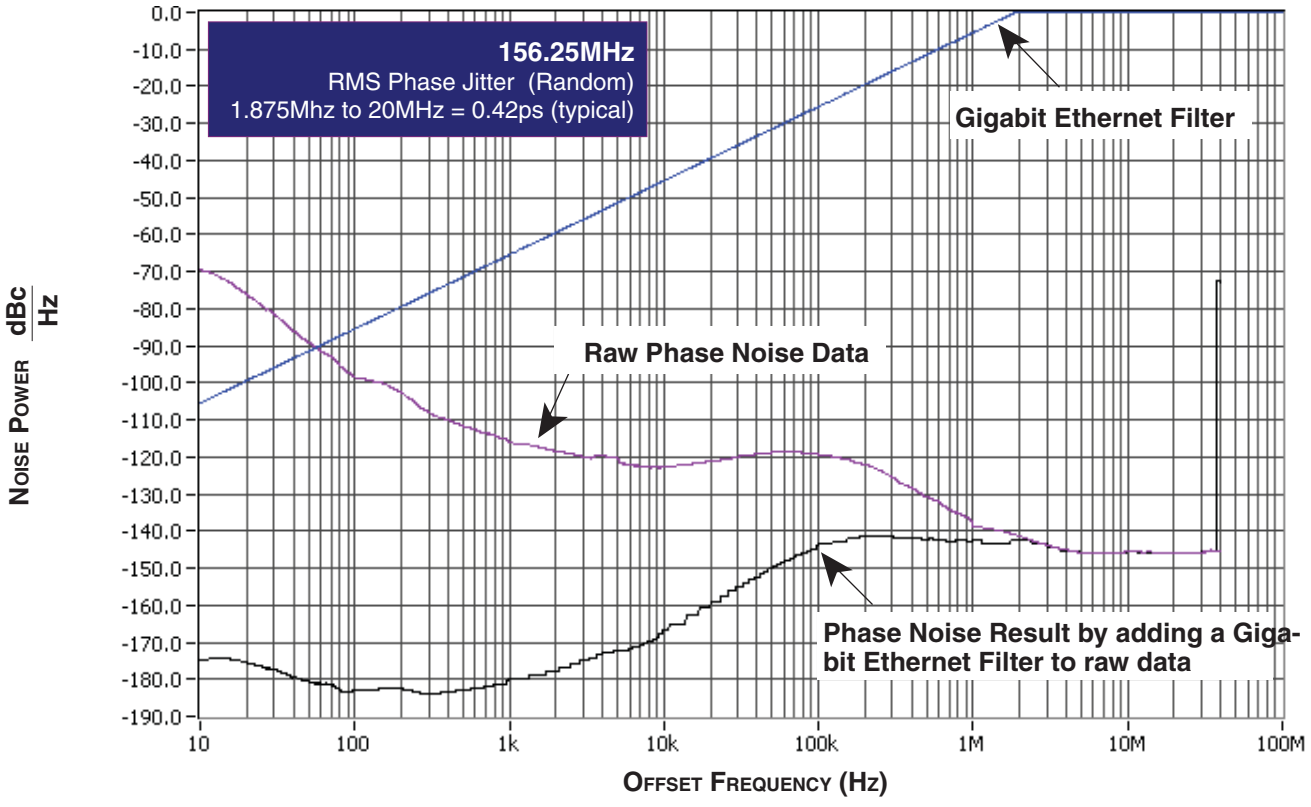
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FSEL = 0		156.25		MHz
		FSEL = 1		125		MHz
tsk(o)	Output Skew; NOTE 1, 2				110	ps
tjit(cc)	Cycle-to-Cycle Jitter				25	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, (1.875MHz - 20MHz)		0.38		ps
		156.25MHz, (1.875MHz - 20MHz)		0.42		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

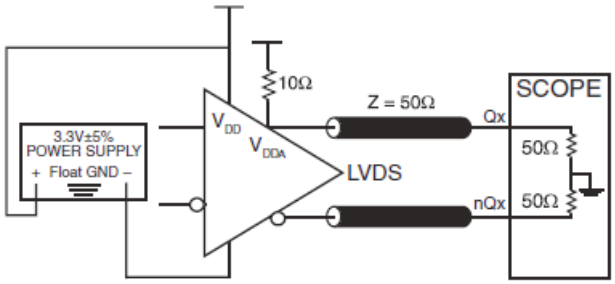
TYPICAL PHASE NOISE AT 125MHZ



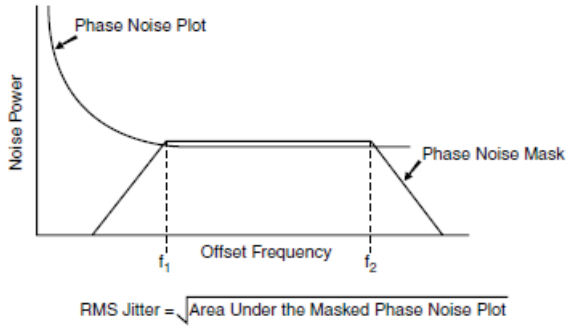
TYPICAL PHASE NOISE AT 156.25MHZ



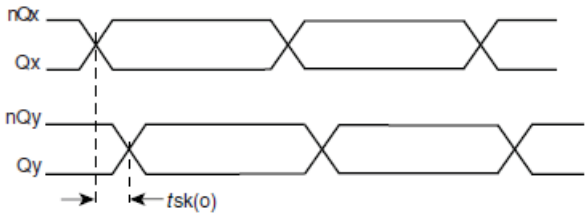
Parameter Measurement Information



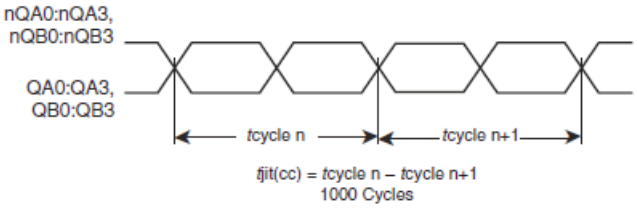
3.3V Core/3.3V Output Load AC Test Circuit



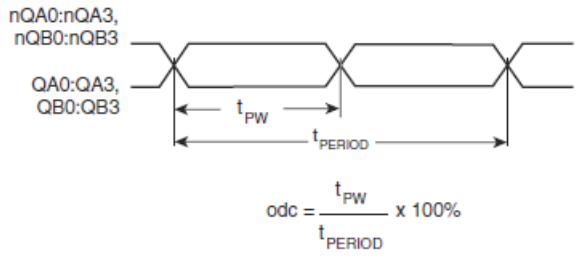
RMS Phase Jitter



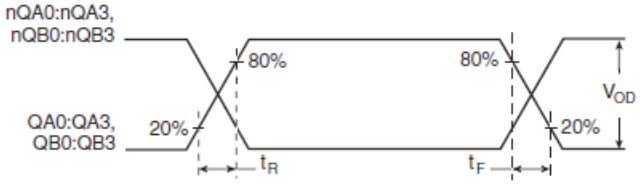
Output Skew



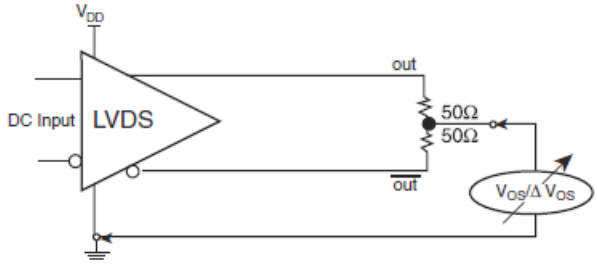
Cycle-to-Cycle Jitter



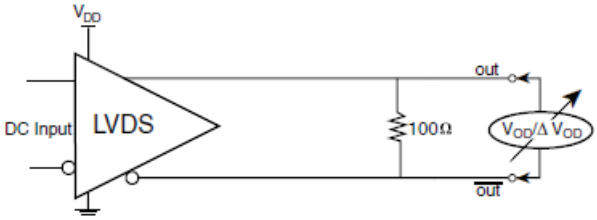
Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844008I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

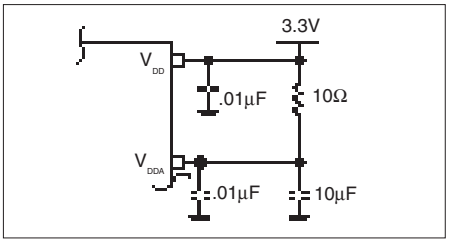


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

Crystal Input Interface

The 844008I-01 has been characterized with an 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz parallel resonant crystal and were chosen to minimize the ppm error.

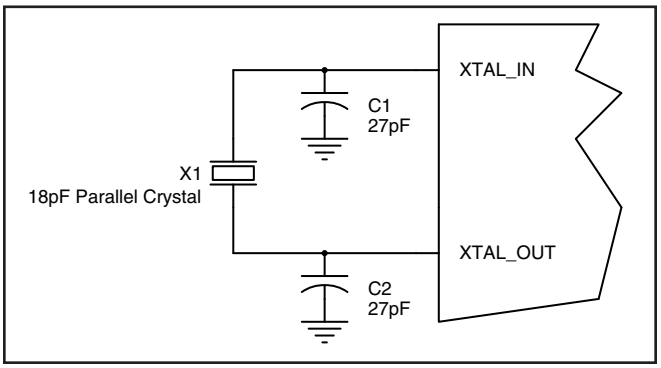


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

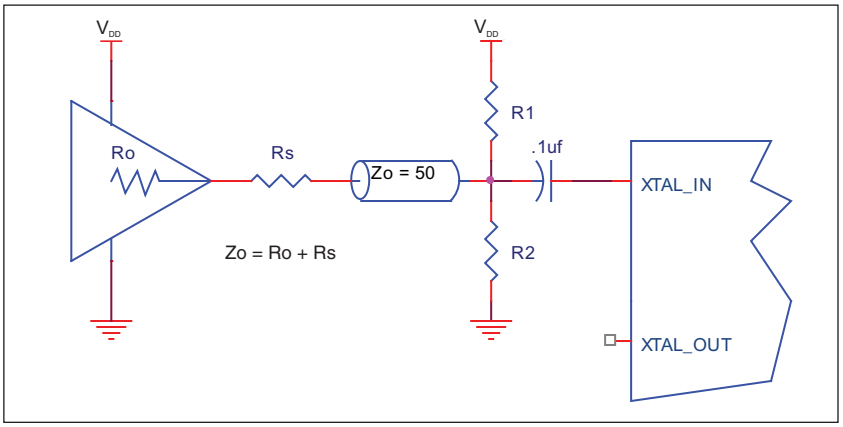


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

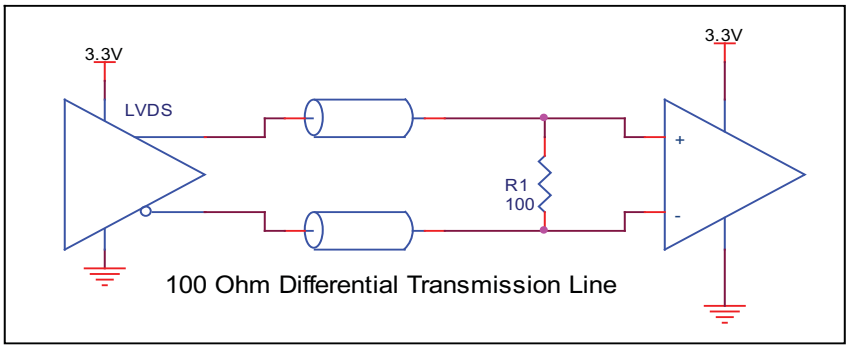


Figure 4. Typical LVDS Driver Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/ shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

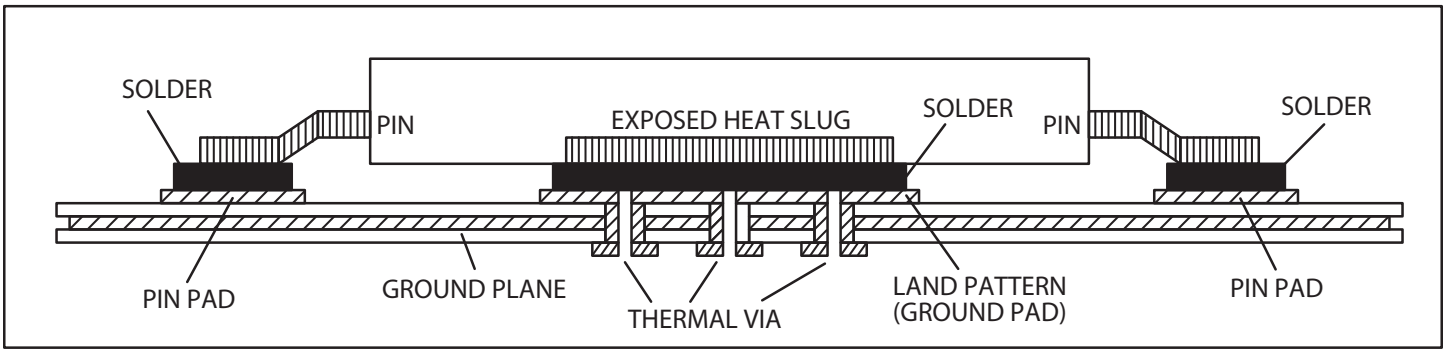


Figure 5. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/ shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

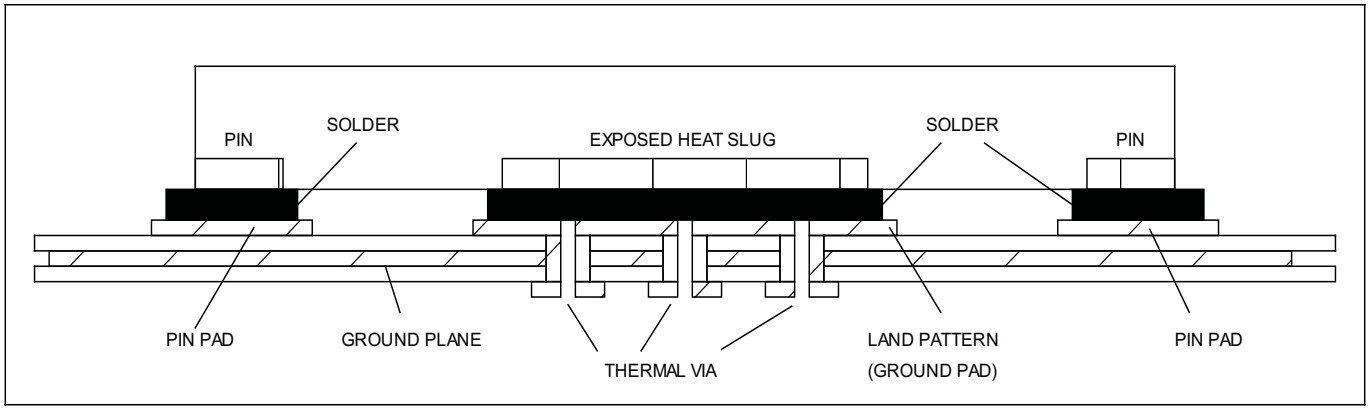


Figure 6. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Schematic Layout

Figure 7 shows an example of 844008I-01 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

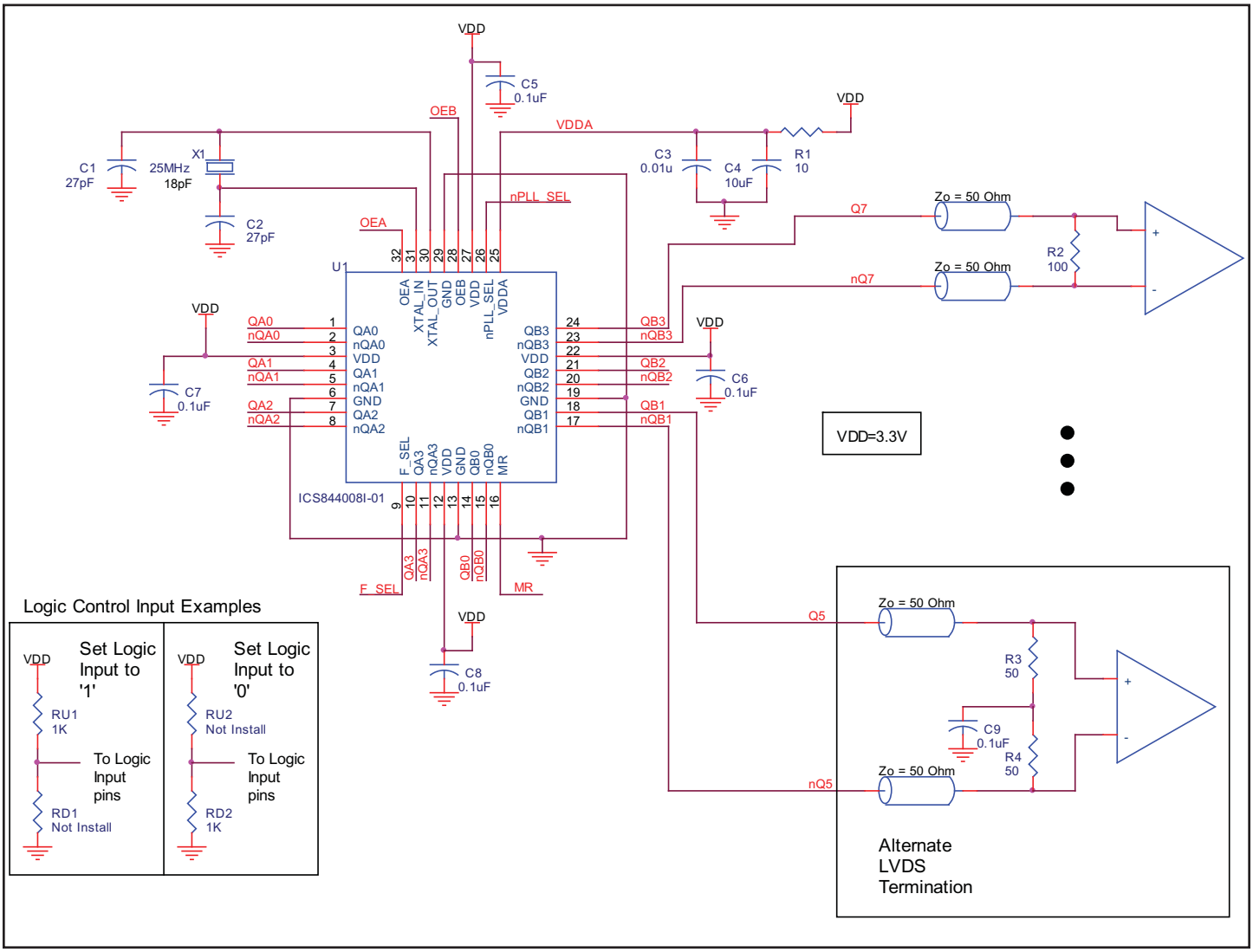


Figure 7. 844008I-01 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 844008I-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 844008I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (275mA + 20mA) = **1022.175mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 1.022W * 37°C/W = 122.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

Table 7A. Thermal Resistance θ_{JA} for 32-Lead TQFP, E-Pad Forced Convection

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

Table 7B. Thermal Resistance θ_{JA} for 32-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for 32 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

Table 8B. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for 844008I-01 is: 2652

Package Outline - Y Suffix for 32 Lead TQFP, E-Pad

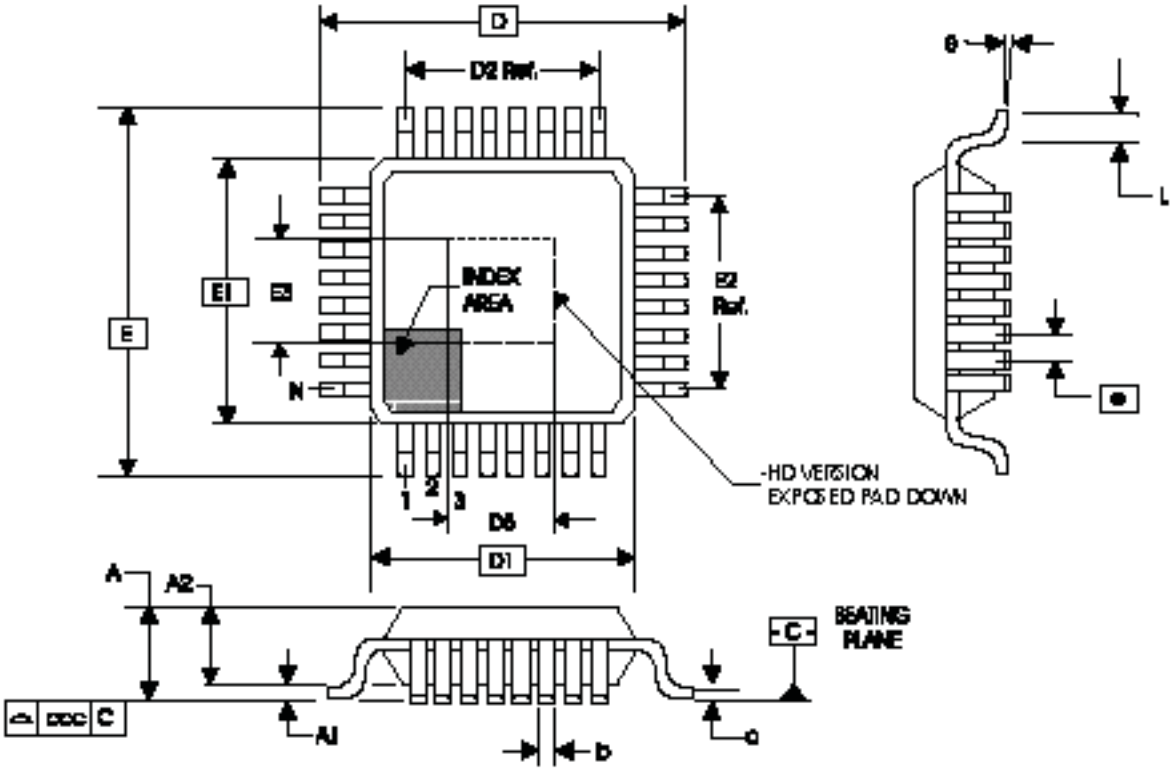
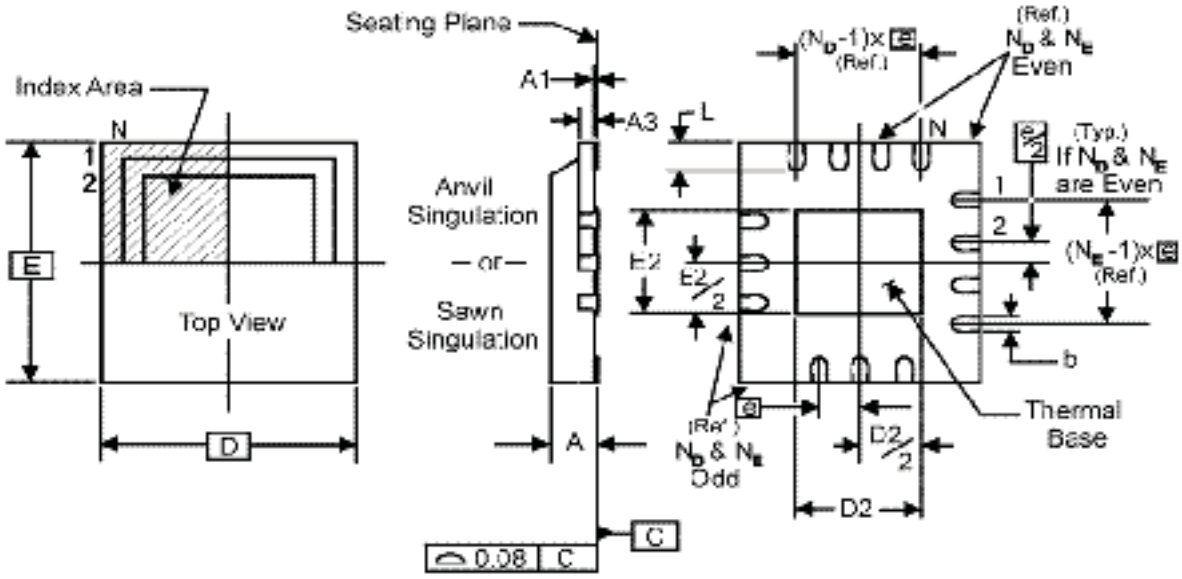


Table 9A. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA-HD		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10
D3 & D3	3.0	3.5	4.0

Reference Document: JEDEC Publication 95, MS-026

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9 below.

Table 9B. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844008AYI-01LF	ICS4008AI01L	32 Lead “Lead-Free” TQFP, E-Pad	Tube	-40°C to 85°C
844008AYI-01LFT	ICS4008AI01L	32 Lead “Lead-Free” TQFP, E-Pad	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T6	4	AC Characteristics Table - corrected cycle-to-cycle jitter limit from 75ps maxmimum to 25ps maximum.	5/13/08
B		10	Added Schematic Layout. Added 32 VFQFN package throughout the datasheet.	11/21/08
B	T10	16	Ordering Information - removed lead free VFQFN package. Updated data sheet format.	4/22/15

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 or +408-284-8200
Fax: 408-284-2775
www.IDT.com

Technical Support
email: clocks@idt.com