# FemtoClock® Crystal-to-LVCMOS/LVTTL Clock Generator

# ICS840022I-02

DATA SHEET

## General Description

The ICS840022I-02 is a Gigabit Ethernet Clock Generator. The ICS840022I-02 uses a 25MHz crystal to synthesize 125MHz or 62.5MHz. The ICS840022I-02 has excellent phase jitter performance, over the 12kHz – 20MHz integration range. The ICS840022I-02 is packaged in a small 16-pin VFQFN, making it ideal for use in systems with limited board space.

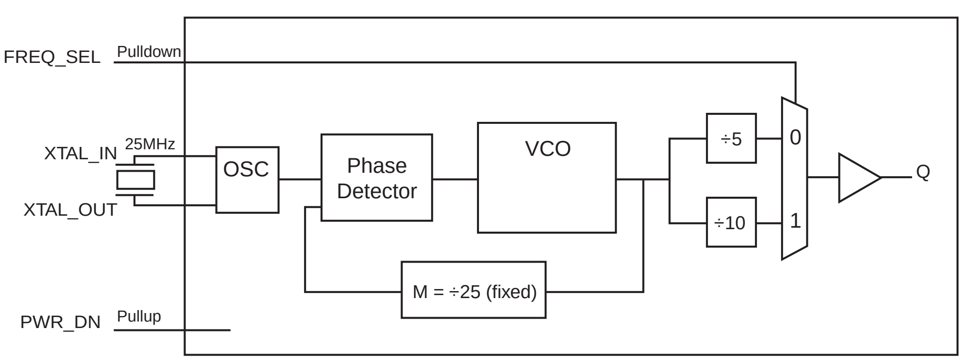
## Features

- One LVCMOS/LVTTL outputs, 20Ω output impedance
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequencies: 125MHz or 62.5MHz
- RMS phase jitter at 125MHz using a 25MHz crystal (12kHz - 20MHz): 0.57ps (typical)
- Supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

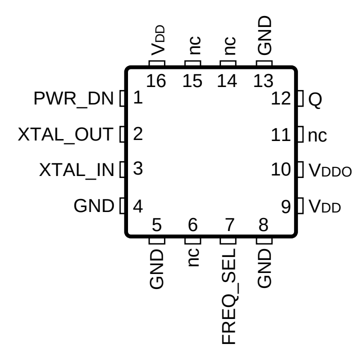
### Function Table

| Inputs | |
|---|---|
| FREQ_SEL | Output Frequency Range (with a 25MHz crystal) |
| 0 | 125MHz |
| 1 | 62.5MHz |

## Block Diagram




## Pin Assignment




**ICS840022I-02**
**16 Lead VFQFN**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | PWR_DN | Input | Pullup | Output state control pin. See Table 3. LVCMOS/LVTTL interface levels. |
| 2,<br>3 | XTAL_OUT,<br>XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 4, 5, 8, 13 | GND | Power | | Power supply ground. |
| 6, 11, 14, 15 | nc | Unused | | No connect. |
| 7 | FREQ_SEL | Input | Pulldown | Frequency select pin. LVCMOS/LVTTL interface levels. |
| 9, 16 | $V_{DD}$ | Power | | Power supply pins. |
| 10 | $V_{DDO}$ | Power | | Output supply pin. |
| 12 | Q | Output | | Single-ended clock output. 20Ω typical output impedance.<br>LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{DD}$, $V_{DD}$ = 3.465V or 2.625V | | 10 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | | | 20 | | Ω |

## Function Table

### Table 3. PWR_DN Function Table

| PWR_DN Input | Description |
|---|---|
| 0 | Output in High-Impedance |
| 1 | Output in normal operation |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 74.9°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | PWR_DN = 1 | | | 77 | mA |
| | | PWR_DN = 0 | | | <1 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 12 | mA |

**Table 4B. Power Supply DC Characteristics,** $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | PWR_DN = 1 | | | 68 | mA |
| | | PWR_DN = 0 | | | <1 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 10 | mA |

**Table 4C. Power Supply DC Characteristics,** $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | PWR_DN = 1 | | | 77 | mA |
| | | PWR_DN = 0 | | | <1 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 10 | mA |

**Table 4D. LVCMOS/LVTTL DC Characteristics,** $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ = 3.465V | 2 | | $V_{DD}$ + 0.3 | V |
| | | | $V_{DD}$ = 2.625V | 1.7 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ = 3.465V | -0.3 | | 0.8 | V |
| | | | $V_{DD}$ = 2.625V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | FREQ_SEL | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| | | PWR_DN | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | FREQ_SEL | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | PWR_DN | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DDO}$ = 3.465V | 2.6 | | | V |
| | | | $V_{DDO}$ = 2.625V | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{DDO}$ = 3.465V or 2.625V | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}$/2. See Parameter Measurement Information, Output Load Test Circuit diagrams.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

## AC Electrical Characteristics

**Table 6A. AC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A$ = -40°C to 85°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | FREQ_SEL = 0 | | 125 | | MHz |
| | | FREQ_SEL = 1 | | 62.5 | | MHz |
| *t*jit(Ø) | RMS Phase Jitter, Random; NOTE 1 | 125MHz, Integration Range: 12kHz – 20MHz | | 0.57 | | ps |
| | | 62.5MHz, Integration Range: 12kHz – 10MHz | | 0.58 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plot.

**Table 6B. AC Characteristics,** $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | FREQ_SEL = 0 | | 125 | | MHz |
| | | FREQ_SEL = 1 | | 62.5 | | MHz |
| *t*jit(Ø) | RMS Phase Jitter, Random; NOTE 1 | 125MHz, Integration Range: 12kHz – 20MHz | | 0.62 | | ps |
| | | 62.5MHz, Integration Range: 12kHz – 10MHz | | 0.58 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

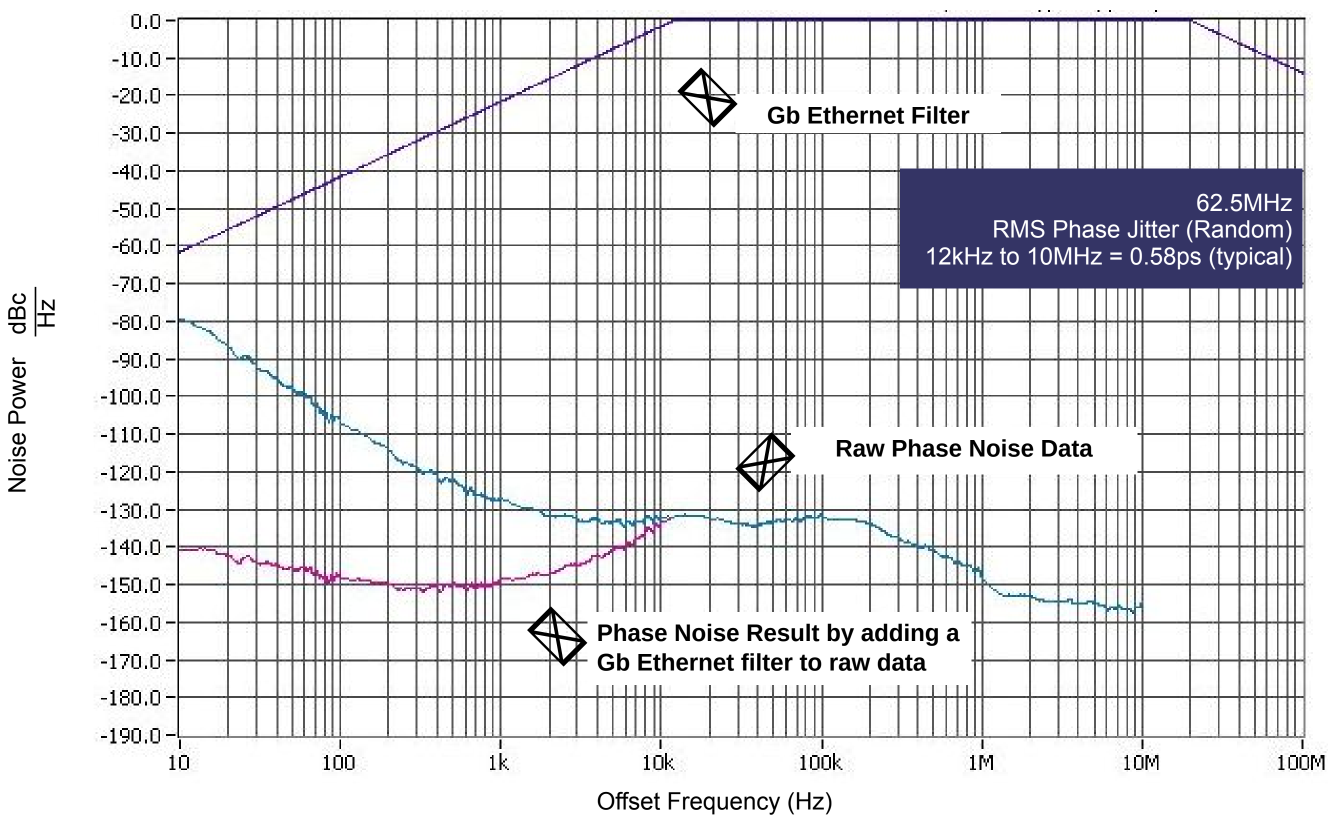
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plot.

**Table 6C. AC Characteristics,** $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°

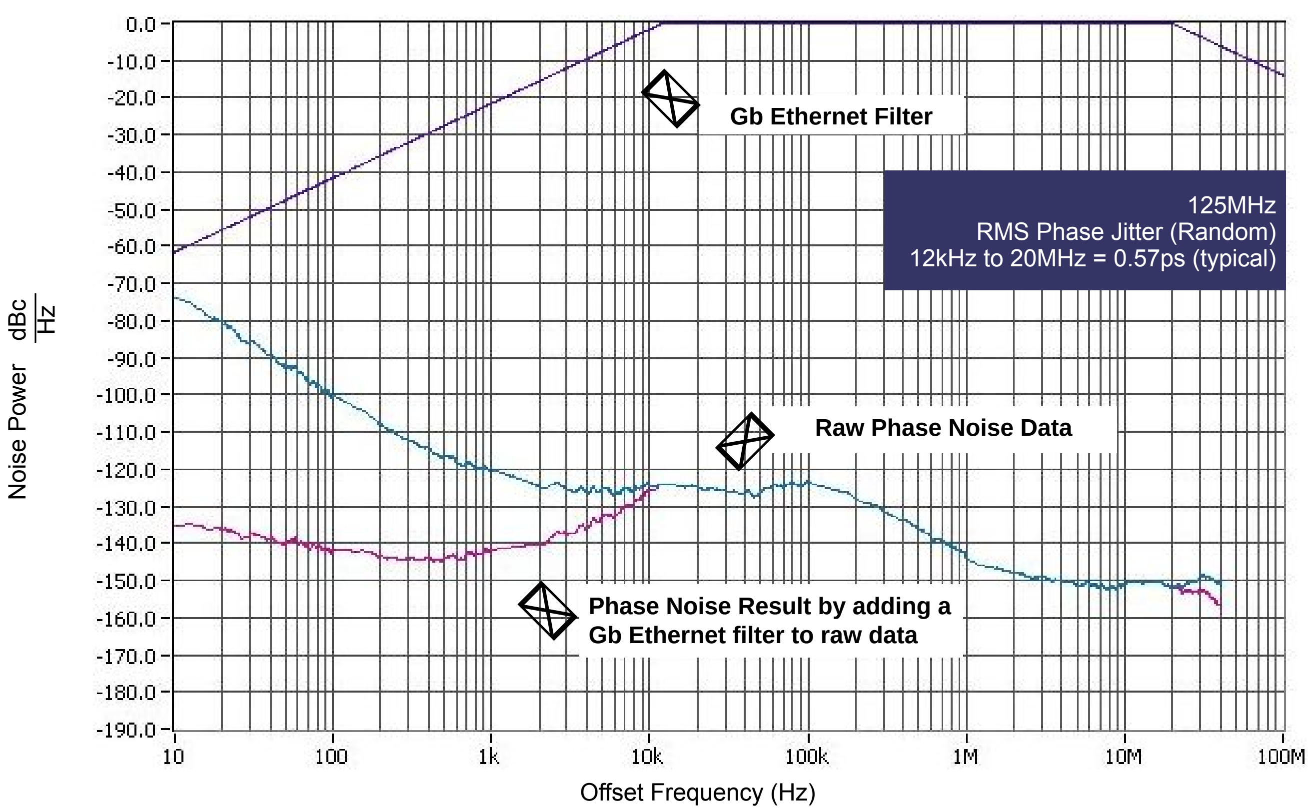
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | FREQ_SEL = 0 | | 125 | | MHz |
| | | FREQ_SEL = 1 | | 62.5 | | MHz |
| *t*jit(Ø) | RMS Phase Jitter, Random | 125MHz, Integration Range: 12kHz – 20MHz | | 0.62 | | ps |
| | | 62.5MHz, Integration Range: 12kHz – 10MHz | | 0.58 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 750 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

## Typical Phase Noise at 62.5MHz (3.3V)

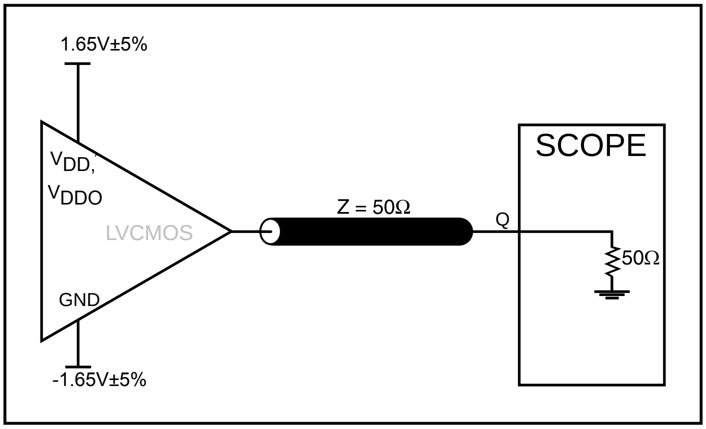



## Typical Phase Noise at 125MHz (3.3V)

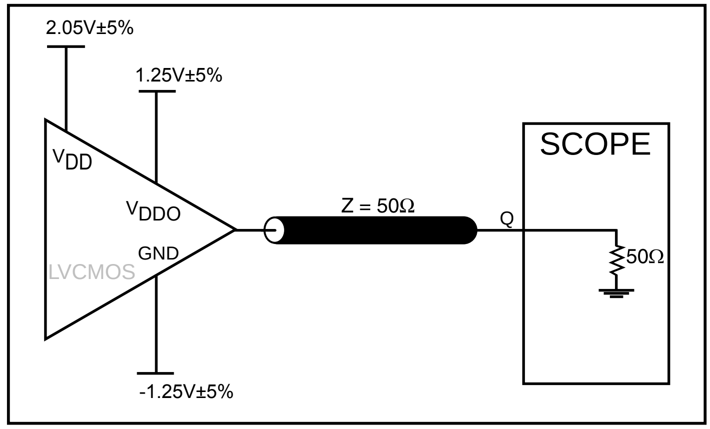


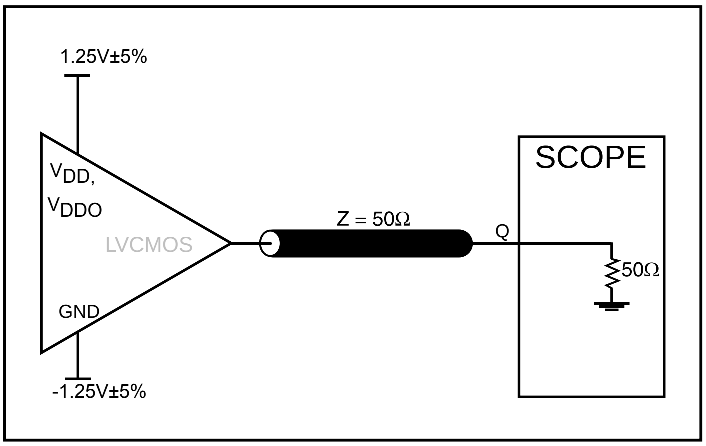
# Parameter Measurement Information



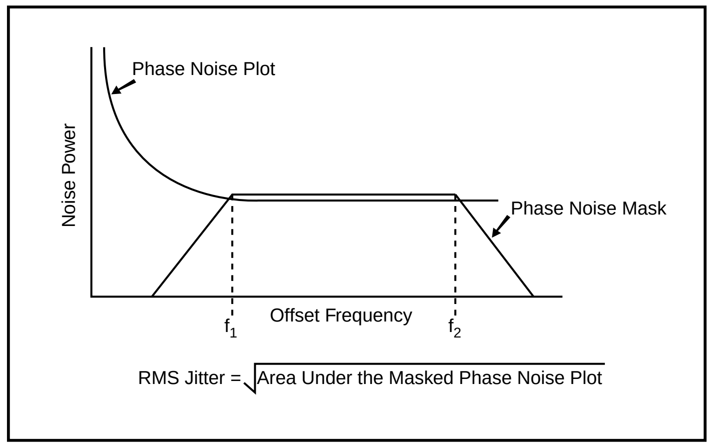

**3.3V LVCMOS Output Load AC Test Circuit**



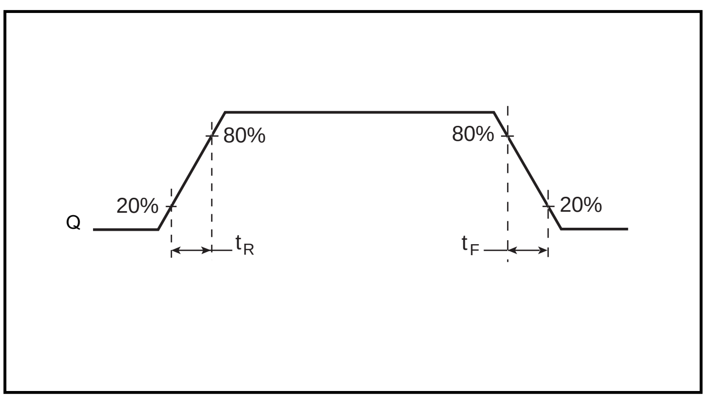

**3.3V/2.5V LVCMOS Output Load AC Test Circuit**



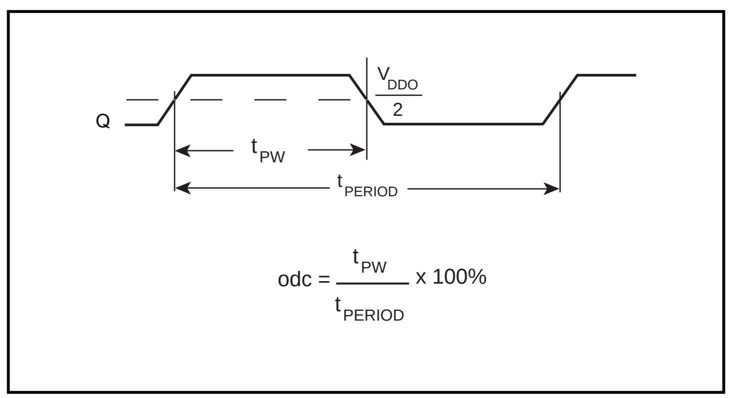

**2.5V LVCMOS Output Load AC Test Circuit**




**RMS Phase Jitter**




**Output Rise/Fall Time**




**Output Duty Cycle/Pulse Width/Period**

# Applications Information

## Crystal Input Interface

The ICS840022I-02 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

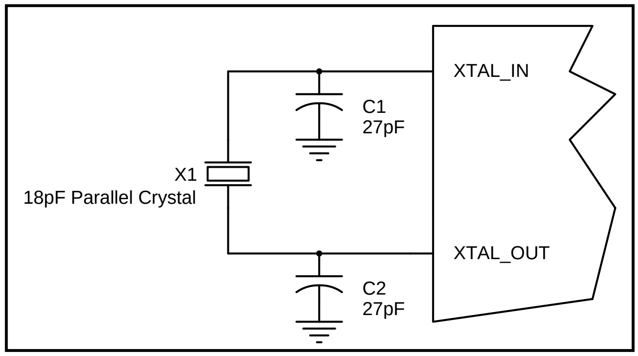



**Figure 2. Crystal Input Interface**

## Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

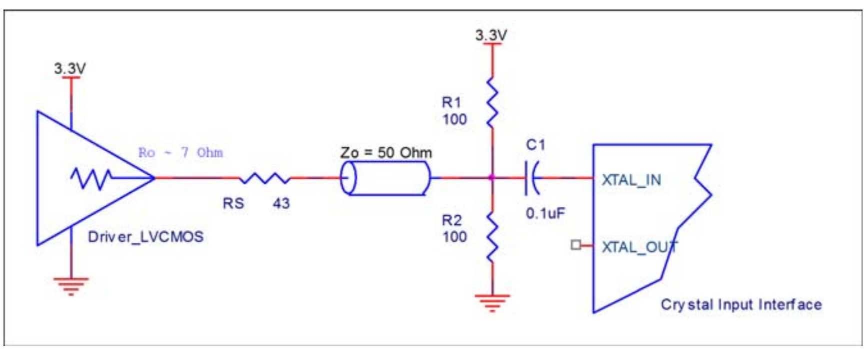



**Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface**

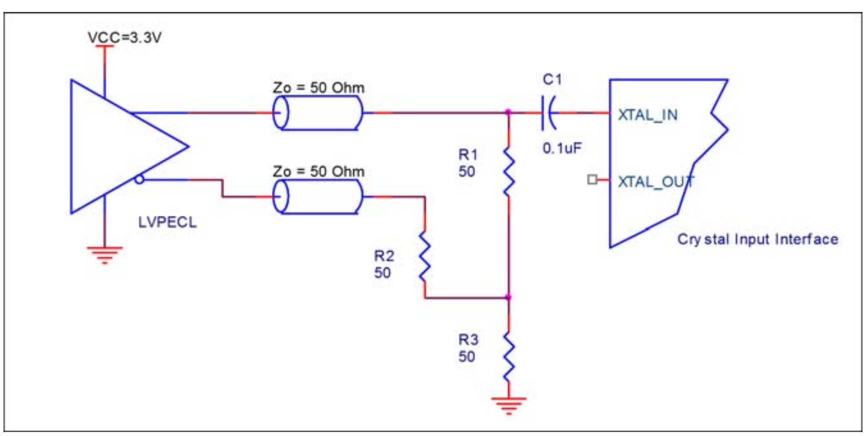



**Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Recommendations for Unused Input Pins

### Inputs:

#### LVCMOS Control Pins

The control pins have an internal pullup and pulldown; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

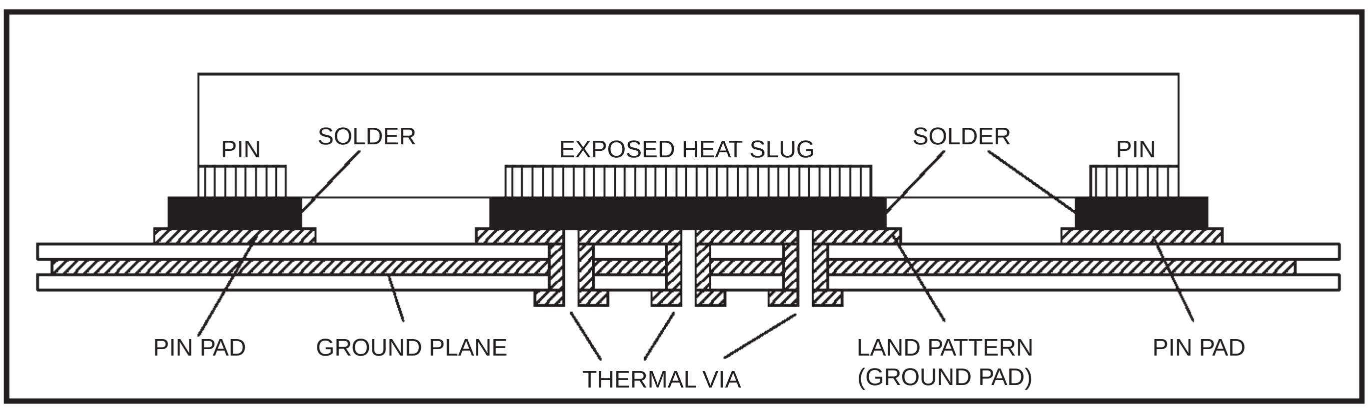



**Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Reliability Information

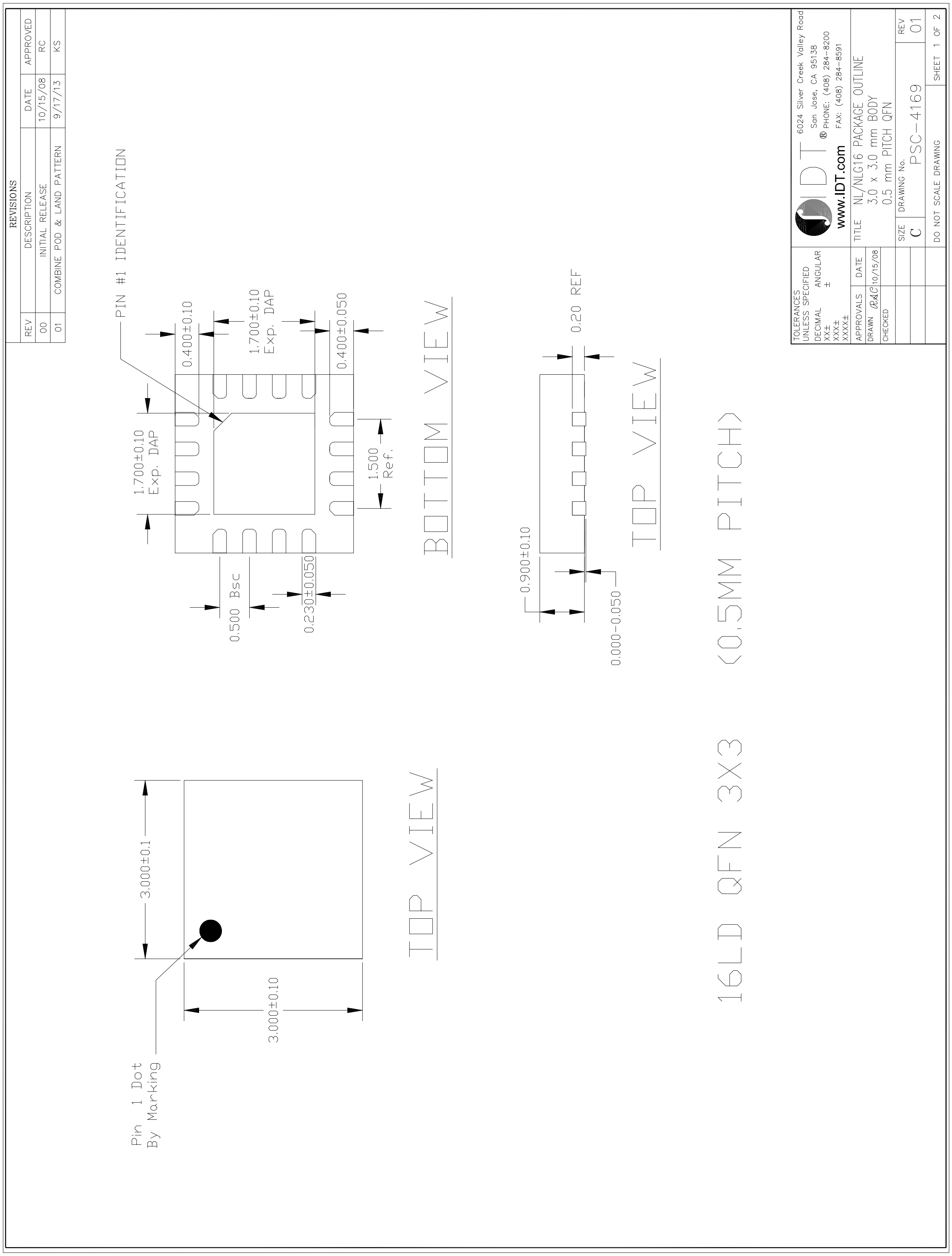
**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 16 Lead VFQFN**

| **$\theta_{JA}$ at 0 Air Flow** | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.9°C/W | 65.5°C/W | 58.8°C/W |

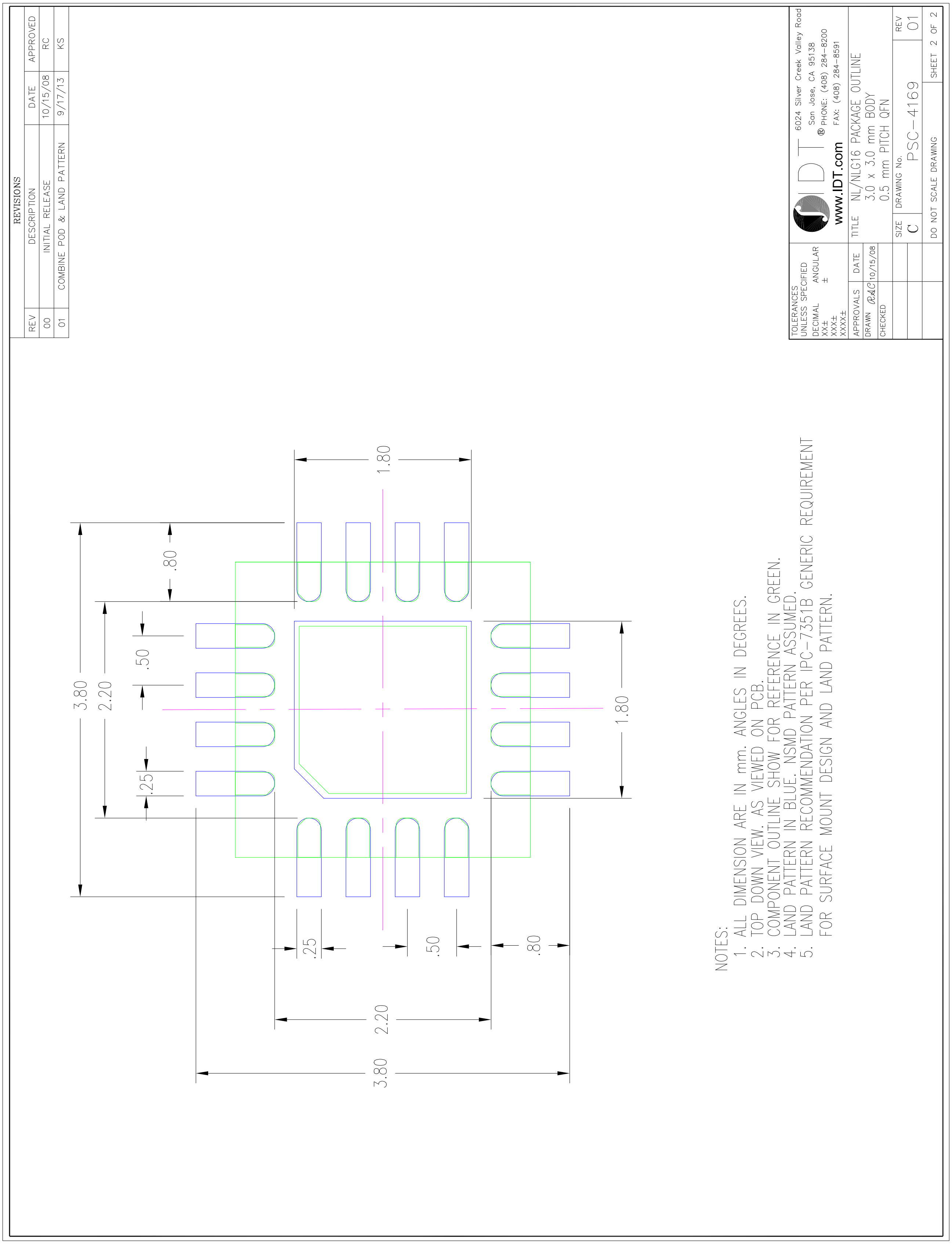
## Transistor Count

The transistor count for ICS840022I-02 is: 1760

# Package Outline Drawings (Sheet 1)



# Package Outline Drawings (Sheet 2)



# Ordering Information

### Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 840022AKI-02LF | 0I2L | "Lead-Free" 16 Lead VFQFN | Tube | -40°C to 85°C |
| 840022AKI-02LFT | 0I2L | "Lead-Free" 16 Lead VFQFN | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | | 1<br>8 | Corrected Block Diagram.<br>Updated VFQFN EPAD Thermal Release Path section. | 11/7/07 |
| B | T4C<br>T6C | 1<br>3<br>5<br>6<br>8<br>11 | Features Section - added 3.3V/2.5V operating supply.<br>Added 3.3V/2.5V Power Supply DC Characteristics Table.<br>Added 3.3V/2.5V Power Supply AC Characteristics Table.<br>Added 3.3V/2.5V Output Load AC Test Circuit diagram.<br>Updated Overdriving the Crystal Interface.<br>Updated Package Drawing.<br>Converted datasheet format. | 7/28/10 |
| B | T9 | 12 | Ordering Information Table - corrected marking from "012L" to "0I2L". | 9/27/10 |
| C | - | 11/12 | Updated the package outline drawings. | 5/27/2017 |

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