

T1/E1 CLOCK MULTIPLIER

ICS548-05

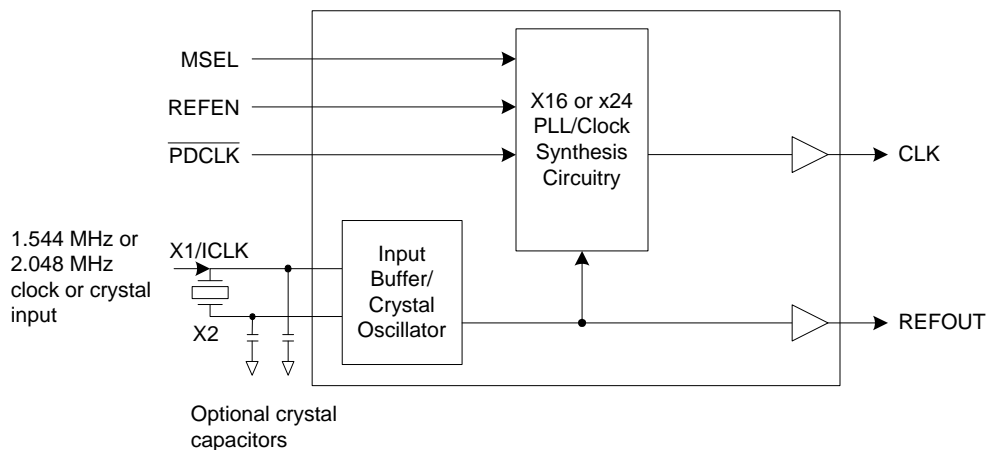
Description

The ICS548-05 is a low-cost, low-jitter, high-performance clock synthesizer designed to produce x16 and x24 clocks from T1 and E1 frequencies. Using IDT's patented analog/digital Phase-Locked Loop (PLL) techniques, the device uses a crystal or clock input to synthesize popular communications frequencies. Power down modes allow the chip to turn off completely, or the PLL and clock output to be turned off separately.

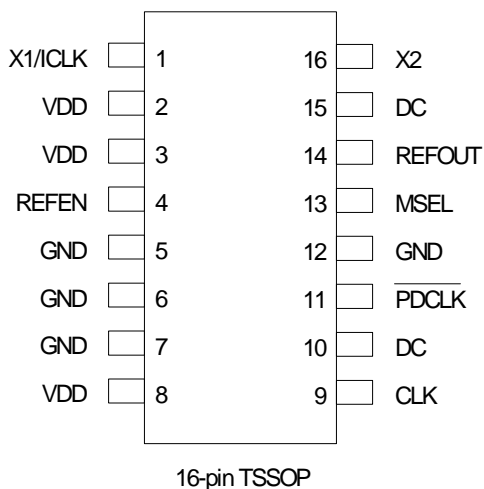
IDT manufactures the largest variety of communications clock synthesizers for all applications. Consult IDT to eliminate VCXO's, crystals, and oscillators from your board.

Features

- Packaged in 16-pin TSSOP
- Available in Pb (lead) free package
- Ideal for telecom/datacom chips
- Replaces oscillators
- 3.3 V or 5 V operation
- Uses a crystal or clock input
- Produces 24.704, 37.056, 32.768, or 49.152 MHz
- Includes Power-down features
- Advanced, low-power, sub-micron CMOS process
- See also the MK2049-34 for generating
- Industrial temperature range available

Block Diagram


Pin Assignment



Output Clock Selection Table

| MSEL | Input (MHz) | CLK (MHz) |
|---------------|---------------------|--------------|
| Pin 13 | Plns 1, (16) | Pin 9 |
| 0 | 1.544 | 24.704 |
| 1 | 1.544 | 37.056 |
| 0 | 2.048 | 32.768 |
| 1 | 2.048 | 49.152 |

Power Down Clock Selection Table

| REFEN | PDCLK | Power Down Selection Mode |
|--------------|---------------|---------------------------------------|
| Pin 4 | Pin 11 | |
| 0 | 0 | The entire chip is off. |
| 0 | 1 | PLL and clock output run, REFOUT low. |
| 1 | 0 | REFOUT running, PLL off, CLK low. |
| 1 | 1 | All running. |

Key: 0 = connect directly to GND; 1 = connect directly to VDD

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|-------------|----------|----------|--|
| 1 | X1/CLK | XI | Crystal connection. Connect this pin to a crystal or clock input. |
| 2, 3, 8 | VDD | Power | Connect to +3.3 V or +5 V. All VDD's must be the same. |
| 4 | REFEN | Input | Reference Clock Enable. See table above. Connect to GND for best jitter/phase noise. |
| 5, 6, 7, 12 | GND | Power | Connect to ground. |
| 9 | CLK | Output | Clock output set by input status of MSEL. See table above. |
| 10, 15 | DC | — | Don't Connect. Do not connect these pins to anything. |
| 11 | PDCLK | Input | Power down clock. See table above. |
| 13 | MSEL | Input | Multiplier select pin. Selects x16 when low, x24 when high. |
| 14 | REFOUT | Output | Buffered reference output clock. Controlled by REFEN. |
| 16 | X2 | XO | Crystal connection. Connect this pin to a crystal or leave unconnected for a clock. |

Key: XI, XO = crystal connections; the input pin MSEL must be tied directly to VDD or GND.
For a clock input, connect the input X1 and leave X2 unconnected (floating).

Application Information

Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Decoupling Capacitors

As with any high performance mixed-signal IC, the ICS548-05 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01μF should be connected between each VDD and GND on pins 3 and 5, as close to the device as possible. Other VDD's can be connected to pin 3. If reFOUT is not used, then REFEN should be connected directly to ground.

Crystal Load Capacitors

If a crystal is used, the device crystal connections should include pads for capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. To reduce possible noise pickup, use very short PCB traces (and no vias) between the crystal and device.

The value of the load capacitors can be roughly determined by the formula $C = 2(C_L - 6)$ where C is the load capacitor connected to X1 and X2, and C_L is the specified value of the load capacitance for the crystal. A typical crystal C_L is 18pF, so $C = 2(18 - 6) = 24$ pF. Because these capacitors adjust the stray capacitance of the PCB, check the output frequency using your final layout to see if the value of C should be changed. For a clock input, leave X2 unconnected (floating).

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
- 2) The external crystal should be mounted next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- 3) To minimize EMI and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.
- 4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS548-05. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS548-05. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70° C |
| Ambient Operating Temperature (industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | | 5.5 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|-----------------|-------------------------------------|-----------|-------|-----------|-------|
| Core Operating Voltage | VDD | | 3.15 | | 5.5 | V |
| Input High Voltage | V _{IH} | X1/ICLK pin, clock input only | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | X1/ICLK pin, clock input only | | VDD/2 | (VDD/2)-1 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -4 mA | 2.4 | | | V |
| Output High Voltage | V _{OH} | CMOS level, I _{OH} = -4 mA | VDD-0.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4 mA | | | 0.4 | V |
| Supply Current | IDD | No Load | | 5 | | mA |
| Power Down Supply Current | IDDPD | No Load | | 1 | | µA |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|----------|-----------------------|------|------|------|-------|
| Short Circuit Current | I_{OS} | CLK output | | ±50 | | mA |
| Input Capacitance | | MSEL, PDCLK, REFEN | | 7 | | pF |
| Frequency Synthesis Error | | Both selections | | | 0 | ppm |

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V, Ambient Temperature 0 to +70° C

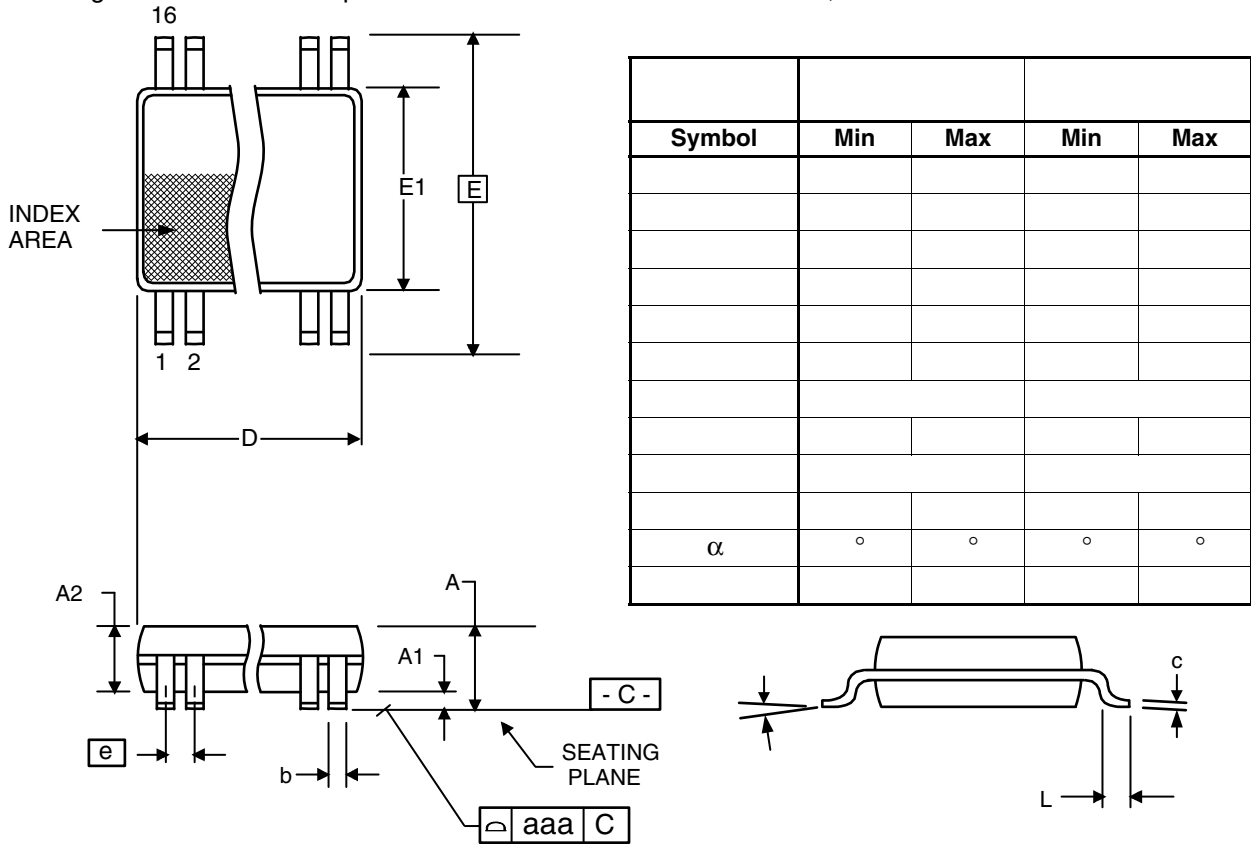
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|----------|-----------------------------------|------|-------------------|------|-------|
| Input Crystal or Clock Frequency | | | | 1.544 or 2.048 | | MHz |
| Output Clock Rise Time | t_{OR} | 20% to 80% | | | 1.5 | ns |
| Output Clock Fall Time | t_{OF} | 80% to 20% | | | 1.5 | ns |
| Output Clock Rise Time | t_{OR} | 20% to 80%, TA = -40 to +85° C | | | 1.7 | ns |
| Output Clock Fall Time | t_{OF} | 80% to 20%, TA = -40 to +85° C | | | 1.7 | ns |
| Output Clock Duty Cycle | t_{OD} | At VDD/2 | 40 | 50 | 60 | % |
| Start-up Time | | VDD = 3.3 V to CLK stable | | | 10 | ms |
| Maximum Absolute Jitter, short term | | | | ±100 | | ps |
| Maximum Absolute Jitter, short term | | TA = -40 to +85° C | | ±150 | | ps |
| One Sigma Jitter | | | | 25 | | ps |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 78 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 70 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 37 | | °C/W |

Package Outline and Package Dimensions (16-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|--------------|---------------|
| 548G-05 | 548G-05 | Tubes | 16-pin TSSOP | 0 to +70° C |
| 548G-05T | 548G-05 | Tape and Reel | 16-pin TSSOP | 0 to +70° C |
| 548G-05LF | 548G05LF | Tubes | 16-pin TSSOP | 0 to +70° C |
| 548G-05LFT | 548G05LF | Tape and Reel | 16-pin TSSOP | 0 to +70° C |
| 548G-05I | 548G-05I | Tubes | 16-pin TSSOP | -40 to +85° C |
| 548G-05IT | 548G-05I | Tape and Reel | 16-pin TSSOP | -40 to +85° C |
| 548G-05ILF | 548G05IL | Tubes | 16-pin TSSOP | -40 to +85° C |
| 548G-05ILFT | 548G05IL | Tape and Reel | 16-pin TSSOP | -40 to +85° C |

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

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