QUAD PLL CLOCK SYNTHESIZER

ICS348-22

Description

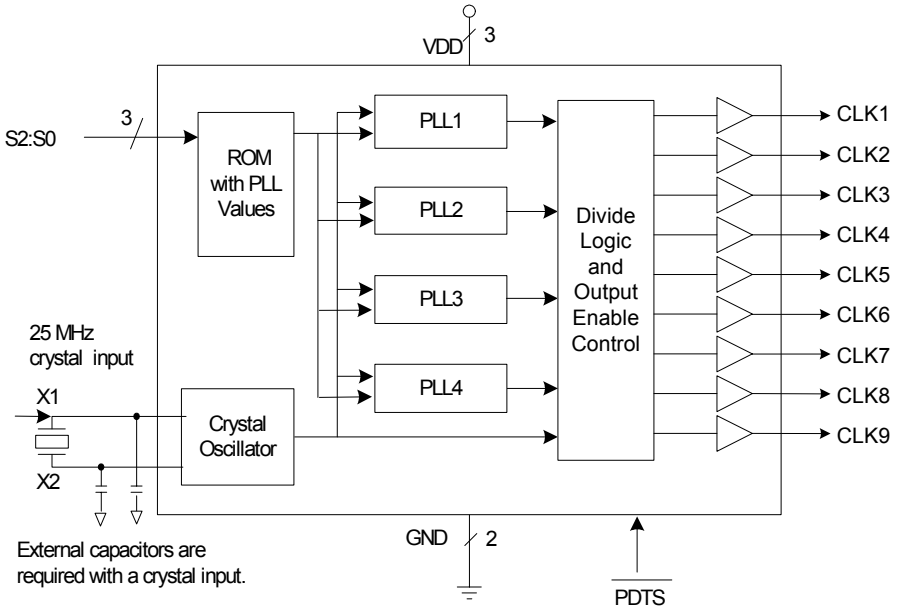
The ICS348-22 synthesizer generates up to 9 high-quality, high-frequency clock outputs including multiple reference clocks from a low frequency crystal or clock input. The ICS348-22 has four independent on-chip PLLs and is designed to replace crystals and crystal oscillators in most electronic systems.

Using Phase-Locked Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

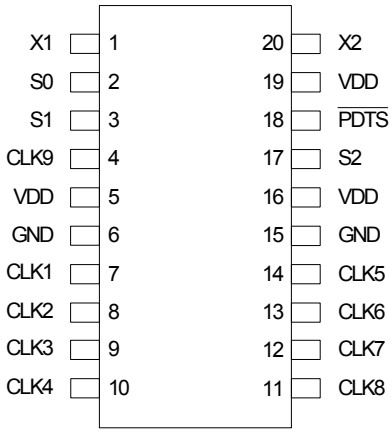
Features

- Packaged as 20-pin SSOP (QSOP)
- Eight addressable registers
- Replaces multiple crystals and oscillators
- Output frequencies up to 189 MHz at 3.3 V
- Input crystal frequency of 25 MHz
- Up to nine reference outputs
- Up to two sets of four low-skew outputs
- Operating voltages of 3.3 V
- Advanced, low power CMOS process
- Available in Pb (lead) free packaging

Block Diagram



Pin Assignment



20-pin (150 mil) SSOP (QSOP)

Output Configuration Table

S2	S1	S0	Outputs
0	0	0	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
0	0	1	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
0	1	0	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
0	1	1	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
1	0	0	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
1	0	1	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
1	1	0	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=187 MHz, CLK8=189 MHz,
1	1	1	CLK1,2,3,4,5,9=127 MHz, CLK6=CLK7=OFF, CLK8=189 MHz,

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Crystal Input. Connect this pin to a 25 MHz crystal.
2	S0	Input	Select pin 0. Internal pull-up resistor.
3	S1	Input	Select pin 1. Internal pull-up resistor.
4	CLK9	Output	127 MHz output clock. Weak internal pull-down when tri-stated
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to ground.
7	CLK1	Output	127 MHz output clock. Weak internal pull-down when tri-stated
8	CLK2	Output	127 MHz output clock. Weak internal pull-down when tri-stated.
9	CLK3	Output	127 MHz output clock. Weak internal pull-down when tri-stated.
10	CLK4	Output	127 MHz output clock. Weak internal pull-down when tri-stated.
11	CLK8	Output	189 MHz output clock. Weak internal pull-down when tri-stated.
12	CLK7	Output	187 MHz output clock. Weak internal pull-down when tri-stated.
13	CLK6	Output	187 MHz output clock. Weak internal pull-down when tri-stated.
14	CLK5	Output	127 MHz output clock. Weak internal pull-down when tri-stated.
15	GND	Power	Connect to ground.
16	VDD	Power	Connect to +3.3 V.
17	S2	Input	Select pin 2. Internal pull-up resistor.
18	$\overline{\text{PDTS}}$	Input	Power down tri-state. Powers down entire chip and tri-states clock outputs when low. Internal pull-up resistor.
19	VDD	Power	Connect to +3.3 V.
20	X2	XO	Crystal Output. Connect this pin to a 25MHz crystal. Float for clock input.

External Components

Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS348-22. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Operating Supply Current Input High Voltage	IDD	Configuration Dependent		TBD		mA
		Nine 33.3333 MHz outs, $\overline{PDTS}$ = 1, no load, Note 1		23		mA
		$\overline{PDTS}$ = 0, no load		20		µA
Input High Voltage	V_{IH}	S2:S0	2			V
Input Low Voltage	V_{IL}	S2:S0			0.4	V
Input High Voltage, $\overline{PDTS}$	V_{IH}		VDD-0.5			V
Input Low Voltage, $\overline{PDTS}$	V_{IL}				0.4	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}			±70		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PUS}	S2:S0, $\overline{PDTS}$		250		kΩ
Internal Pull-down Resistor	R_{PD}	CLK outputs		525		kΩ
Input Capacitance	C_{IN}	Inputs		4		pF

Note 1: Example with 25 MHz crystal input with nine outputs of 33.$\overline{3}$ MHz, no load, and VDD = 3.3 V.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental Crystal		25		MHz
Output Frequency		VDD=3.3 V	0.25		189	MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		1		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1		ns
Duty Cycle		Note 2	40	49-51	60	%
Power-up time		PLL lock-time from power-up, Note 3		3	10	ms
		$\overline{\text{PDTS}}$ goes high until stable CLK output, Note 3		0.2	2	ms
One Sigma Clock Period Jitter		Configuration Dependent		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from Mean. Configuration Dependent		±200		ps
Pin-to-Pin Skew		Low Skew Outputs	-250		250	ps

Note 1: Measured with 15 pF load.

Note 2: Duty Cycle is configuration dependent. Most configurations are minimum 45% and maximum 55%.

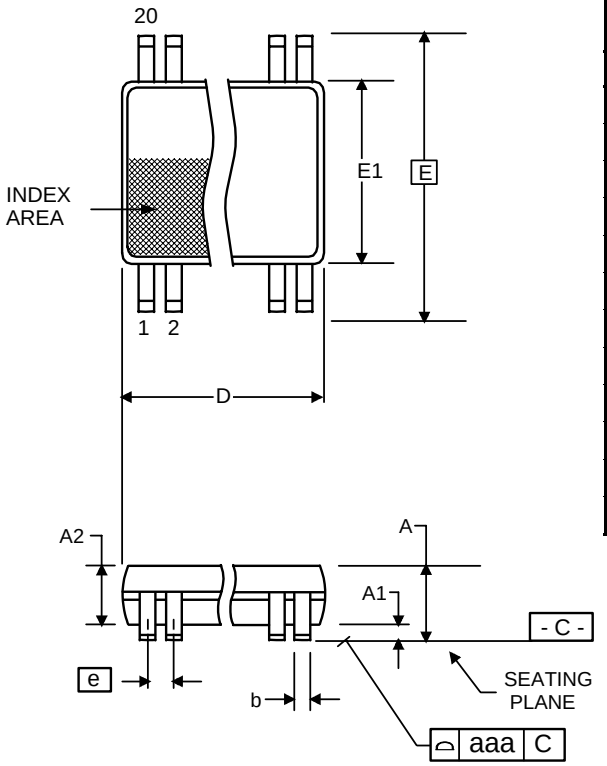
Note 3: ICS test mode output occurs for first 170 clock cycles on CLK7 for each PLL powered up. $\overline{\text{PDTS}}$ transition high on select address change.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
348R-22	ICS348R-22	Tubes	20-pin SSOP	0 to +70° C
348R-22T	ICS348R-22	Tape and Reel	20-pin SSOP	0 to +70° C
348R-22LF	ICS348R22LF	Tubes	20-pin SSOP	0 to +70° C
348R-22LFT	ICS348R22LF	Tape and Reel	20-pin SSOP	0 to +70° C

"LF" denotes Pb (lead) free package.

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