Integrated Device Technology, Inc.

FCT-T OCTAL LOGIC CHARACTERISTICS AND APPLICATIONS

APPLICATION NOTE AN-152

By Stanley Hronik

INTRODUCTION

IDT FCT Octal Logic is form, fit, and function compatible with other industry standard logic families, but will provide a significant performance improvement in most applications. IDT's FCT Octal Logic is available in a variety of configurations, allowing the designer to select the proper component for the application.

This application note is intended to be used as a designer's guide to component selection and usage. The data contained within this document is typical data taken at 25ºC and 5.0V Vcc, except where otherwise noted. The data has been derived from component characterization where in most cases, the component selected is a '244 type. The data is intended as a design guideline only. For "guaranteed" specifications the IDT Logic Data Book provides full specifications over Vcc, temperature and process.

TABLE OF CONTENTS

OCTAL LOGIC FAMILIES

IDT's Octal Logic includes several families, each with specific target applications. Consistent among all of the families is the high speed and very low power dissipation. Pin and functionality uniformity is maintained across the families, allowing plug in replacement if a family transition is required. All FCT logic comes in a variety of speed grades, allowing plug in replacement for performance upgrades or a downgrade for cost savings. The speed grades are uniform across all FCT families including the 16 bit Double Density and 3.3V families.

The Octal FCT Logic families can be divided into three distinct groups:

1) FCTxxxT, High Drive
2) FCT2xxxT, Balanced Drive
3) FCTxxx, CMOS Drive

High Drive has TTL level outputs with -15/64mA drive capability. High Drive is intended for driving heavily loaded busses and backplanes where significant current levels are required. The TTL level outputs, give lower noise levels and faster switching speeds than can be obtained with similar CMOS rail swing components. High drive has Power-off Disable, making the family ideal for partially powered applications or situations where an interface may become connected/disconnected while powered.

Balanced Drive Octals also have TTL level outputs with a drive capability of -15/12mA. Internal series resistors on Balanced Drive reduce the drive and noise levels, giving superior low noise performance on moderately to lightly loaded busses. The series resistors provide source termination, eliminating the need for external series resistors in most applications. Balanced Drive is ideal as a general use family.

The CMOS output components have full rail to rail output voltage swing with TTL level input thresholds. These components are intended only for applications requiring the CMOS rail swing output voltages. The High Drive and Balanced Drive TTL level components with lower voltage switching levels will provide higher performance, lower noise, and lower dynamic power dissipation.

Gate Array Design Approach

FCT logic is built using standard gate arrays with a "sea of gates". The arrays are uniform across products of similar pin count, but allow a final metal mask variation which gives the unique part type logic characteristics. In addition, the final metal mask allows a selection of output characteristics, allowing a single array type to provide all families including High Drive, Balanced Drive and CMOS.

Using the standard gate array approach, IDT maintains a high level of consistency from component to component and logic family to logic family. This eases component qualification for most users because a single qualification makes available a wide variety of products.

DC ELECTRICAL CHARACTERISTICS

Included in the DC Electrical Characteristics are device

input and output impedances, drive capabilities and breakdown limitations. The guaranteed DC test limits are shown in the IDT Logic Data Book in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table and OUTPUT DRIVE CHARACTERISTICS table for each component. When calculating loading, drive capabilities, power dissipation and line termination needs, additional information beyond the data book specifications is often required. This information is supplied here.

Input Characteristics

The input structure of all IDT FCT logic is shown in Figure 1. The structure consists of the gates to a P-Channel and an N-Channel FET. A parasitic clamp diode connects the input to ground, but there is no clamp diode to Vcc associated with the input. Components that combine an input with an output (forming an I/O port) may have a clamp to Vcc depending upon the type of output structure selected.

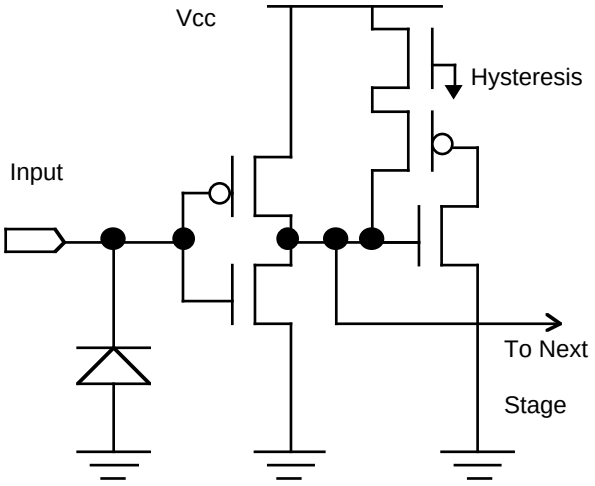

Figure 1, Input Structure

Contained within the input structure is a hysteresis circuit that provides a weak positive feedback into the input causing a small difference between Vih (logic HIGH threshold) and Vil (logic LOW threshold). This helps to reduce noise induced switching and oscillations that may occur when the input voltage level hovers near the input toggle point.

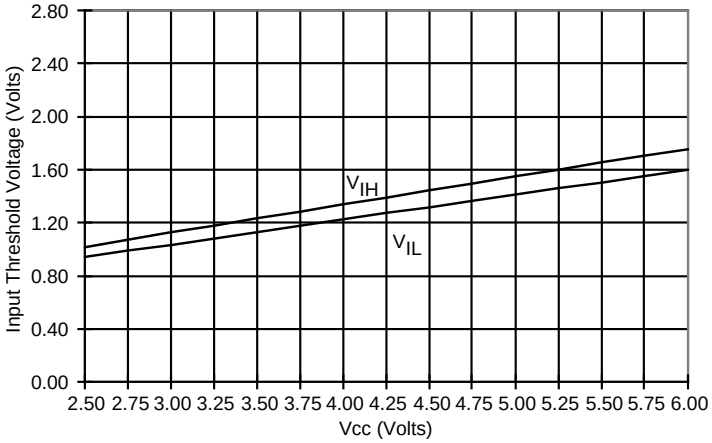

Figure 2, Input Threshold Voltage (Vih/Vil)

The input threshold voltage for FCT-T logic is set at a nominal 1.5V with Vcc = 5.0V. As can be seen in Figure 2, the input threshold will vary relative to Vcc with the input hysteresis causing the slight difference between Vih and Vil. The data sheet limit for Vil is >0.8V and the limit for Vih is <2.0V. These values are guaranteed when Vcc is between 4.5V and 5.5V.

Figure 3 shows the V/I curve for device inputs. As the input voltage drops below -0.7V the effect of the input clamp can be seen as the input current level increases dramatically. Within the normal operating range of -0.5V to 5.5V, the input current typically is <0.1uA. As the input voltage increases beyond the absolute maximum rating (7.0V), the device will begin breakdown. This typically occurs at some level beyond 12 volts and may cause damage to the component.

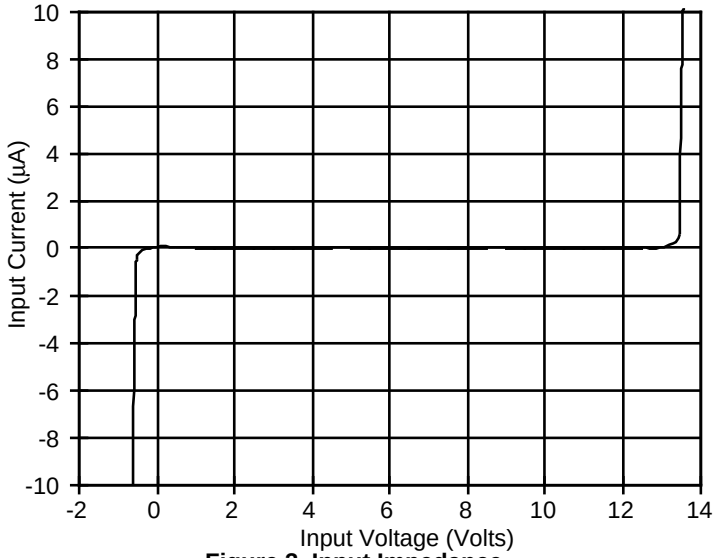

Figure 3, Input Impedance

Unused and Floating Inputs

Because of the high input impedance of CMOS components an input will not drive itself to a valid logic state. Inputs left floating may float near the logic threshold and cause power dissipation as shown in Figure 29. In addition, if the input is picking up a low level, high frequency noise, the input stage may toggle causing the component to oscillate. If the oscillating frequency becomes extreme, the power dissipation of the component may reach high levels, eventually causing device failure.

Special problems may occur with inverting components that have floating inputs. As a floating input toggles the device, the reverse direction of the output switching on an inverter may cause a temporary shifting of the ground reference (ground bounce). A change in ground reference may change the input toggle voltage, causing it to pass back through the floating input voltage. As this back and forth ground shifting continues, the device may go into a high frequency oscillation.

Input hysteresis which is present on all FCT logic should mitigate many of the oscillation effects caused by noise on a floating input, slowly rising/falling input signals, and bounce, but a typical 200mV hysteresis level is not sufficient to fully overcome these effects.

Unused inputs should be tied directly to Vcc or GND to

achieve very low input power dissipation. Using a pull up or pull down resistor of any value (<100KΩ) is also acceptable. Rising and falling input levels of greater than 5 to 10ns should be avoided to insure clean transitions. Slowly rising edges (as may be seen with a large pull up/down resistor) may not produce clean output waveforms, but will cause no component damage.

Output Characteristics

Since all of the FCT Octal Logic is built using standard gate arrays, device characteristics are uniform across families except for the output structure which is unique for each family. Each family is adapted to provide superior performance in a range of applications. High Drive with a low output impedance is ideally suited to driving heavy busses and backplanes. Balanced Drive is ideal for driving on board busses, memory arrays, and other circuits that require low noise levels. CMOS Drive is adapted for circuits that require the higher voltage swing of CMOS.

High Drive Output Structure

The High Drive output structure is shown in Figure 4. The impedance values shown include the impedance of the associated FET in saturation. The pull down impedance which is approximately 6.5Ω is capable of driving a 64mA load without exceeding a Vol level of 0.55 volts.

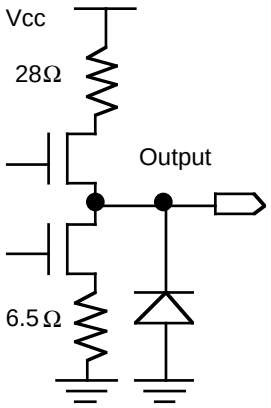

Figure 4, FCTxxxT Output Structure

Figure 5 shows the pull down impedance of a High Drive Octal. Saturation is reached at approximately 260mA with Vol > 2.5V.

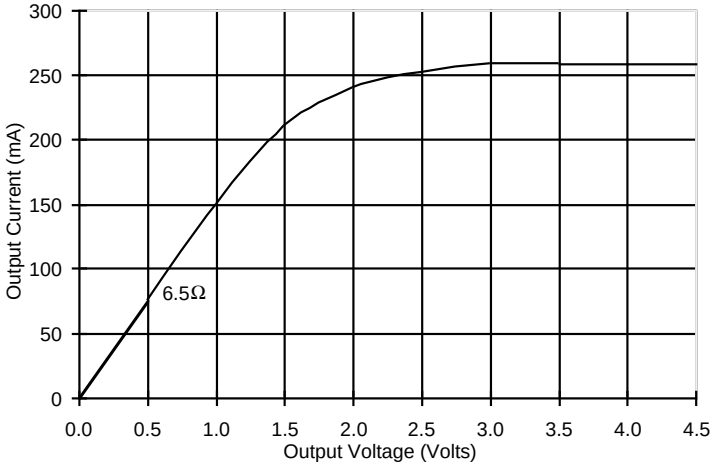

Figure 5, VOL Characteristics of High Drive

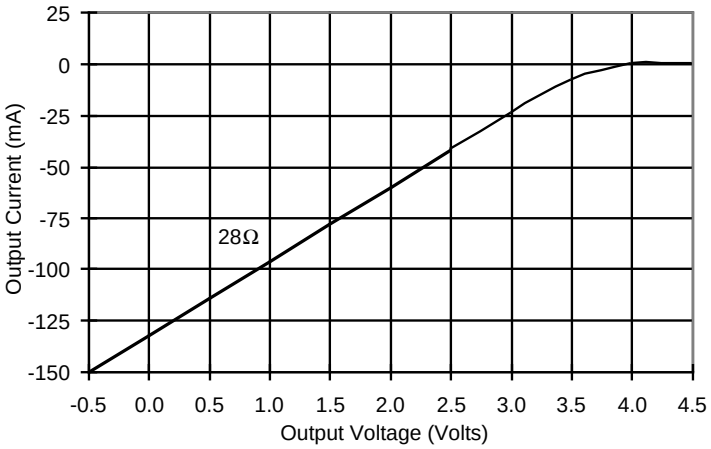

Figure 6, VOH Characteristics of High Drive

Figure 6 shows the pull up impedance for the same component. Saturation is not reached within the test range of -0.5V to 4.5V, but cut off is seen at approximately 3.5V. Cut off is due to the requirement for a gate to source voltage drop of approximately 1.5V to turn the pull up N-Channel FET on. The point of cut off will vary directly with the value of Vcc. Using this voltage drop from Vcc is how TTL logic levels are achieved in CMOS components. For a typical case then, a High Drive component can be modeled as a 6.5Ω resistor to ground for a logic LOW and a 28Ω resistor to 3.5V (Vcc - 1.5V) for a logic HIGH.

High Drive has no clamp diode between either the output or input to Vcc, giving the component “Power-off Disable” capability. Power-off Disable allows use of the component in partially powered or hot insertion applications. A full description of the feature and design techniques can be found in Application Note #AN-158.

Balanced Drive Output Structure

FCT2xxxT logic contains larger integrated series resistors as shown in Figure 7. These resistors significantly reduce ground bounce, line noise, EMI, and other deleterious effects of excessive drive. The impedance values shown include the saturation impedance of the FETs.

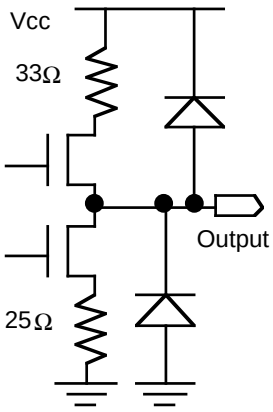

Figure 7, FCT2xxxT Output Structure

Because of the clamp diode between Vcc and the device output, Balanced Drive cannot be used in Power-off Disable applications. Raising the device output beyond Vcc will forward bias the clamp diode and possibly cause a burnout of the device. The inputs on Balanced Drive have no clamp and therefore can be tied to a powered bus while Vcc is off.

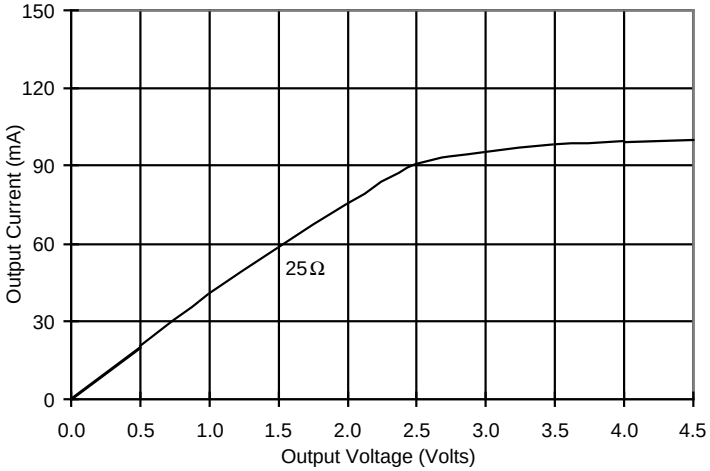

Figure 8, Vol Characteristics of Balanced Drive

Comparing Figure 8 with Figure 5 it can be seen that the Balanced Drive has a higher pull down impedance than High Drive. It should be noted this would approximate an 18.5Ω resistor in series with a High Drive output for the pull down. This will provide a light series termination, but it may be desirable to add additional resistance if the application requires a fine tuning of the output impedance. The advantage of a slightly lower output impedance is the ability to drive a heavier load while maintaining speed. Also first incident wave switching is easier to achieve with a lower output impedance.

The graph of Figure 9 shows the output high characteristics of Balanced Drive. As can be seen in the chart, the pull up impedance is only slightly higher than a High Drive component. This will soften the rising edge of the output signal, but still give a good clean edge. Usually the rising edge of a N-Channel driven signal is not a significant source of noise, therefore the lower impedance will help maintain the faster propagation delay of the component. This effect gives a significant benefit in a series termination application where a Balanced Drive component is used instead of a High Drive with an external series resistor.

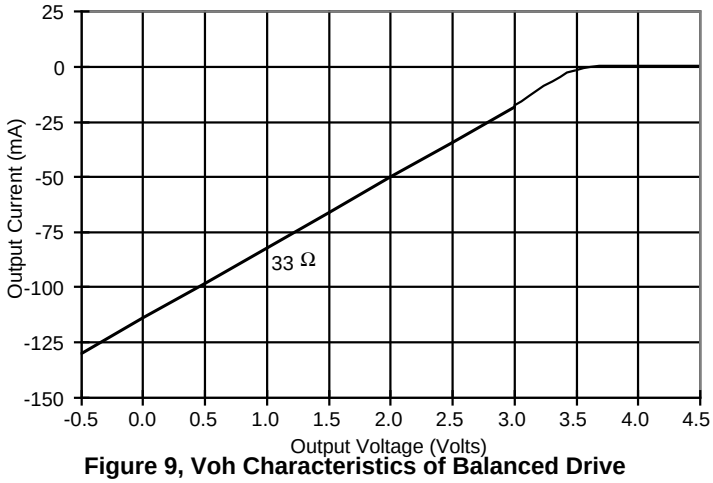

Figure 9, Voh Characteristics of Balanced Drive

The impedance of an I/O port for Balanced Drive in 3-state is shown in Figure 15. As shown in the figure, the effect of the clamp diodes to Vcc on the device output will limit the range of the input voltage.

CMOS Drive Output Structure

FCTxxx CMOS components have a pull down structure similar to the FCTxxxT High Drive. The pull up structure though is far different, containing a P-Channel FET as shown in Figure 10, instead of the N-Channel which is characteristic of the TTL level components. The P-Channel pull up will drive the output voltage to Vcc for a logic HIGH state.

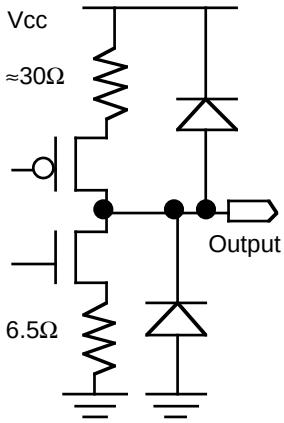

Figure 10, CMOS Drive Output Structure

The Vol characteristics of the CMOS devices are shown in Figure 11. As can be seen by the figure, the pull down impedance is about 6.5Ω which is similar to High Drive. The two components have essentially the same pull down structure.

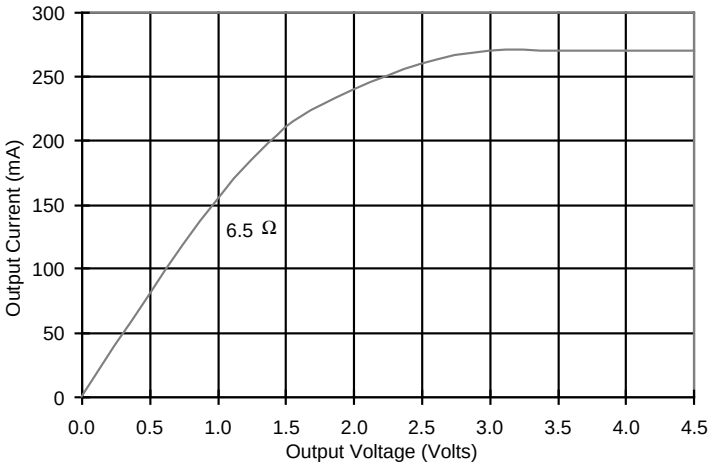

Figure 11, CMOS Output Low Characteristics

The pull up characteristics of FCT CMOS are shown in Figure 12. Because of the P-Channel pull up, the output pulls to the Vcc rail (nominally 5.0V) and the output impedance curve is not as flat as is seen with N-Channel devices. By drawing a line from 5V to 1.5V (as shown in Figure 12), the impedance of a logic HIGH can be approximated at 30Ω

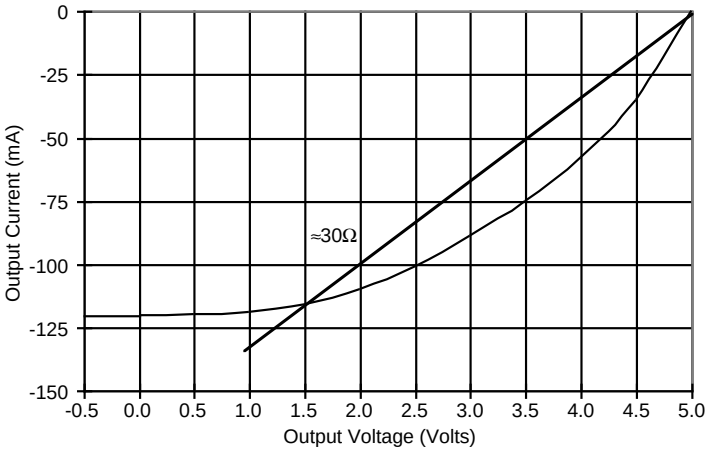

Figure 12, CMOS Voh Characteristics

CMOS Drive components have a clamp diode between the device output and Vcc as shown in Figure 10. This clamp does not allow these components to be used in Power-off Disable applications. Like Balanced Drive though, the device inputs don't have a clamp and can be used in partially powered or hot insertion applications.

The impedance of an I/O port for CMOS in 3-state is shown in Figure 15. As shown in the figure, the leakage currents on an I/O port are minimal until the input/output voltage passes beyond the level necessary to forward bias the clamp diodes.

Comparison with Double Density

For completeness, the characteristic pull up and pull down structures of the FCT Double Density components are shown in Figure 13. The Octal High Drive output is very similar to the High Drive Double Density. The Octal Balanced Drive output drive is positioned at a mid point between Double Density Balanced Drive and Double Density BD-Lite. There are no Double Density CMOS rail swing components.

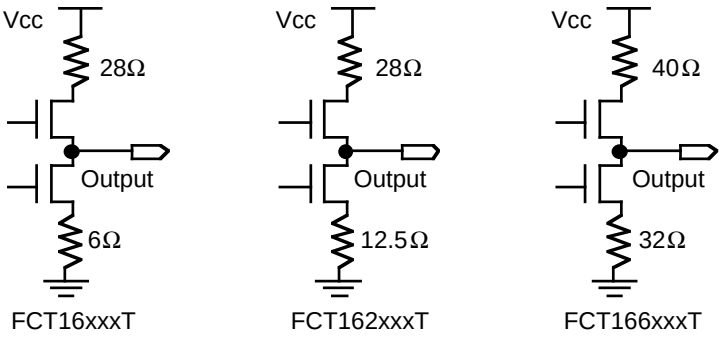

Figure 13, Double Density Output Structures

Connecting Outputs Together

Occasionally in an application where a very strong drive is needed, it is possible to connect two outputs together to double the drive capability of the device as shown in Figure 14. When connecting outputs together certain rules must be followed to prevent potentially damaging the component output structure.

- The two outputs must be from the same component.
- The two outputs should be adjacent pins and shorted with a trace between the two pins.
- The two inputs should be shorted with a trace between the two pins.
- The two outputs must always have the same state (for instance a counter may toggle state and destroy itself).

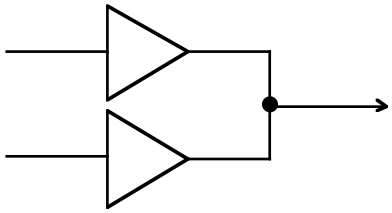

Figure 14, Connecting Outputs Together

Bus Contention

FCT logic cannot be used to perform any type of wire 'OR' or 'AND' dot functions except when using open drain devices. FCT logic is designed for high performance and has drive levels that are sufficiently strong to cause damage either to the FCT component or other devices on the bus in the case of sustained bus contention or wire 'OR' operations.

A common system design error is attempting to identify possible bus contention situations by calculating bus timings using "worst case" propagation delays on some components combined with "best case" propagation delays on others. Worst case is found under hot, low Vcc conditions while best case is found under cold, high Vcc conditions. These two conditions are not usually combined in a system, meaning that it is not practical to attempt to calculate system timings using best and worst case conditions within the same timing calculations.

Output disable times are shorter than output enable times in FCT devices, avoiding bus contention when switching with common control signals. In addition, the data book times for both tend to be somewhat lengthy compared to typical delays.

Brief periods of bus contention during switching consisting of a 1 to 2 ns contention during switching should not cause device damage in most cases. During contention the power dissipation will rise to very high levels, possibly causing overheating if the contention is frequent or a significant portion of the duty cycle. Lengthy bus contention of several nsec that may develop from a high speed device such as an FCT being enabled simultaneously with a slow speed device such as an HCT being disabled, may cause device damage.

I/O Port Characteristics

I/O Ports are simple combinations of input and output structures on the same pin. When acting as an output driver, an I/O port will have identical characteristics to a standard unidirectional output port from the same family. When the output driver is 3-stated (High Z) the port will be acting as an input port. When using Balanced Drive or CMOS Drive components, the output clamp diode to Vcc will limit the range of the input voltage to Vcc + 0.5V as shown in Figure 15. High Drive I/O ports will have identical characteristics to a unidirectional input port when the output is 3-state.

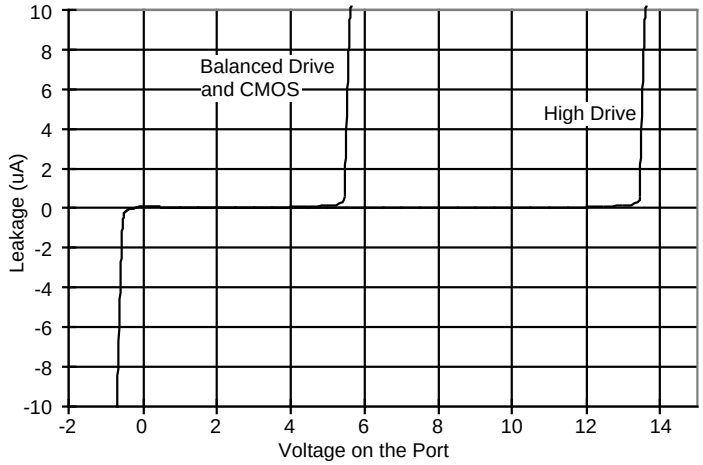

Figure 15, Leakage on an I/O Port in a High Z State

Power-off Disable is possible on any port that allows the pin voltage to rise above Vcc without forward biasing clamp diodes. As seen in Figure 15, High Drive allows the pin voltage to rise above Vcc, giving High Drive the Power-off Disable capability on I/O ports. Balanced Drive and CMOS clamp the I/O port to Vcc, limiting the output voltage to Vcc + 0.5V. Therefore Balanced Drive and CMOS Drive do not have Power-off Disable capability on their I/O ports.

AC Electrical Characteristics

The FCT logic families are very high performance and are stable under a wide variety of conditions. The AC specifications for each component are available in the "SWITCHING CHARACTERISTICS OVER OPERATING RANGE" table in the data sheet for each component. There are a few things that do affect AC performance which need to be addressed. These include Vcc level, loading, and temperature.

Delay as a Function of Supply Voltage

Component propagation delay is sensitive to changes in Vcc. Typically higher Vcc levels will increase component speed and reduce propagation delays. An occasional exception to this is the HIGH to LOW transition which may increase in speed due to a lower starting voltage (Voh).

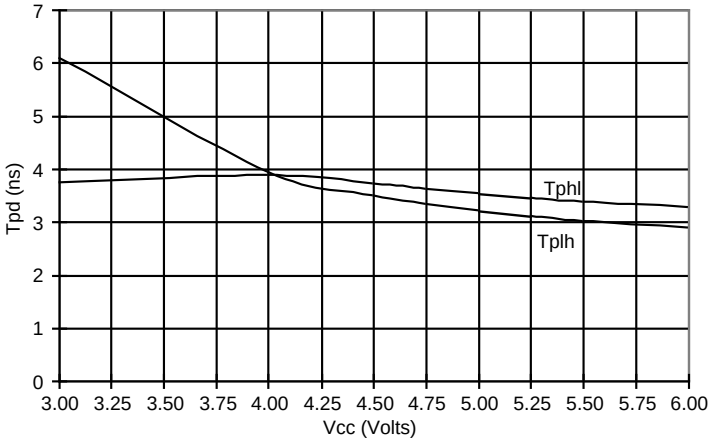

Figure 16, Tpd vs. Vcc (High Drive)

Figure 16 shows the effect of Vcc on the propagation delay of an Octal High Drive component. The propagation delay is fairly linear in the normal operating range, but as Vcc lowers significantly it can be seen that pull up begins to have difficulty achieving the logic high condition.

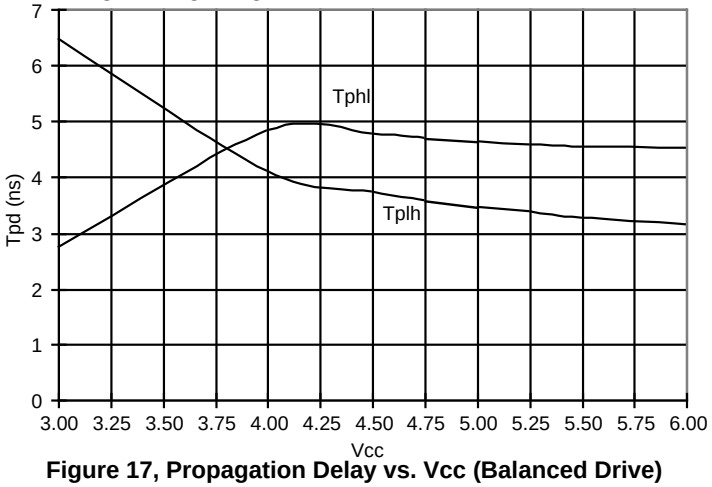

Figure 17, Propagation Delay vs. Vcc (Balanced Drive)

The Octal Balanced Drive of Figure 17 shows that the HIGH to LOW transition tends to be longer than the LOW to HIGH. The increased output impedance of Balanced Drive has greater difficulty driving a load and therefore the propagation delay is increased for this transition. The effect on the Tphl is more pronounced than Tplh because the voltage transition from a HIGH to the threshold point is greater than the transition from a LOW to the threshold point. In addition the Balanced Drive pull down is weaker than the pull up, while for a High Drive the reverse is true.

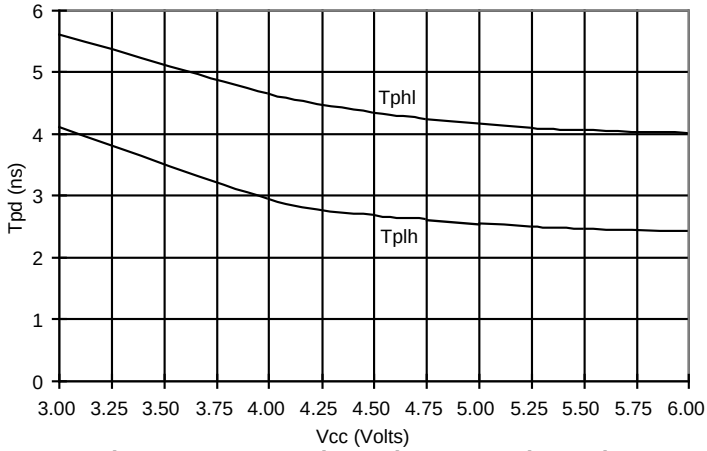

Figure 18, Propagation Delay vs. Vcc (CMOS)

The CMOS rail swing component of Figure 18 shows a significant difference between Tphl and Tplh. The transition voltage as seen in the Balanced Drive is also an effect here. A HIGH to LOW transition must travel from 5.0V to 1.5V (=3.5V total) to register as a LOW, while a LOW to HIGH must travel only from 0V to 1.5V (=1.5V total) to register as a logic HIGH.

Performance Under Temperature

Propagation delay will vary with changes in temperature. Typically these variations are small compared to variations in Vcc, but they are present and do have an effect. As the temperature rises, the propagation delay will increase. As the temperature lowers, the component will demonstrate improved speed performance.

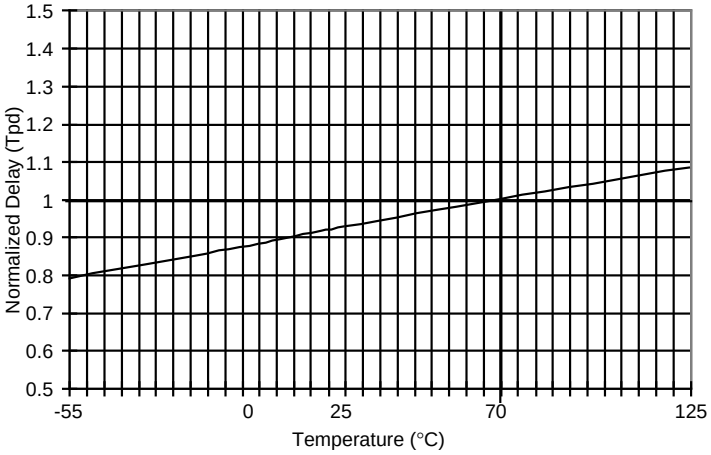

Figure 19, Normalized Delay vs. Temperature

Figure 19 shows how the propagation delay will vary with temperature. The variation is fairly consistent regardless of component family (Balanced Drive, High Drive and CMOS).

The data book specifications are guaranteed between 0º and 70ºC for most octal logic components. To ease calculations, Figure 19 has been normalized to 70ºC. The data book limits have been set for testing purposes only and do not imply a failure to operate outside of these ranges. FCT logic will operate easily at -55ºC, but may exhibit performance levels faster than the data sheet limits. The maximum temperature on the component die should be limited to 150ºC beyond which component degradation may occur (metal migration). The die temperature will be affected by both the ambient temperature and the component power dissipation. Die temperature can be calculated using the thermal data in section 4 of the IDT Logic Data Book and the POWER SUPPLY CHARACTERISTICS table in each data sheet.

Rise and Fall times

When calculating transmission line effects, it is necessary to know the rise and fall times of the drivers under the intended load. As the load increases, the rise/fall times will increase, reducing the need for line termination. Wherever possible, Balanced Drive should be used to avoid the faster, noisier edge rates.

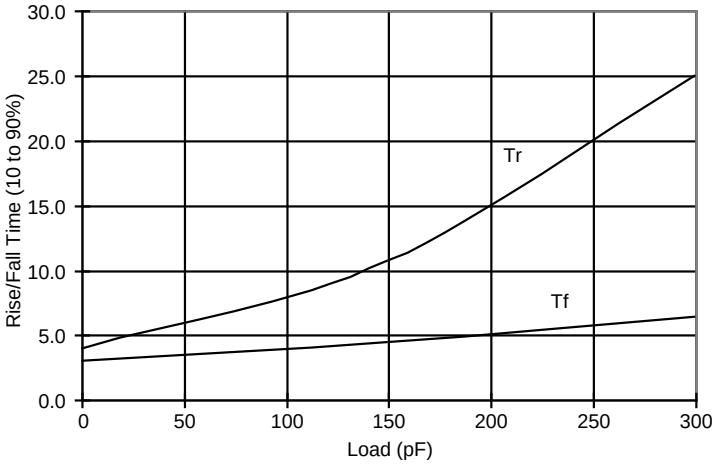

Figure 20, Rise/Fall Time, Hi Drive

The rise and fall times for a standard Octal High Drive component are shown in Figure 20. The higher impedance of the device pull up structure causes the rising edge to be more affected by load than the falling edge from the lower impedance device pull down structure.

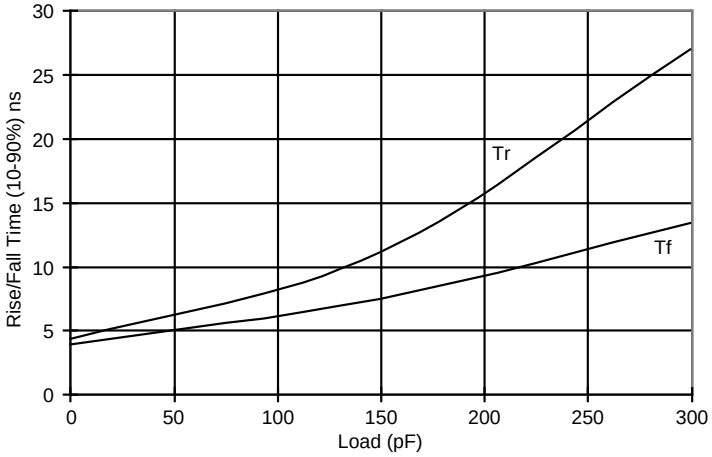

Figure 21, Rise/Fall Balanced Drive

Figure 21 shows the rise/fall time for a Balanced Drive component. The effect of the internal series resistor in the component can be seen as the RC time constant reduces the edge rate as the load increases, particularly in the falling edge.

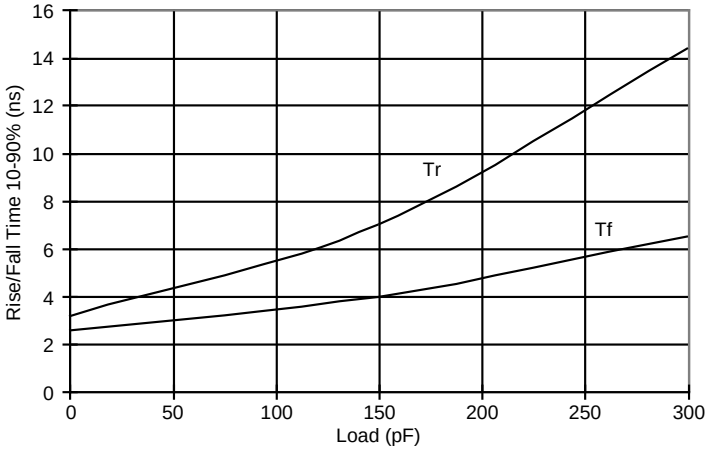

Figure 22, Rise/Fall Time CMOS

Figure 22 shows rise and fall times for the CMOS output components. The falling edge takes longer than a High Drive because the output Voh is higher, causing a larger voltage transition from a HIGH to a LOW. The rising edge is faster than a High Drive, because the logic threshold remains at the 1.5V level even though the output HIGH is being driven to a higher Voh. The edge rate measured in Volts/ns is faster for both the rising and falling edges because of the higher Voh voltage. The higher edge rate of a CMOS output component will generate more line noise than a High Drive or Balanced Drive component.

Delay Vs Load

As the load on an output increases, the effective delay through the component will increase. This is primarily because of the increase in the rise and fall time of the device

output delaying the time the signal will cross the logic threshold. Secondarily the increased load may exceed the current supplying capacity of the component temporarily, adding additional delay while the load charges.

The following examples are for a typical '244 type component. Other components respond similarly except there may be an additional propagation delay due to the normal internal delay of the component. This delay is not affected by load and can be directly added to the increase shown.

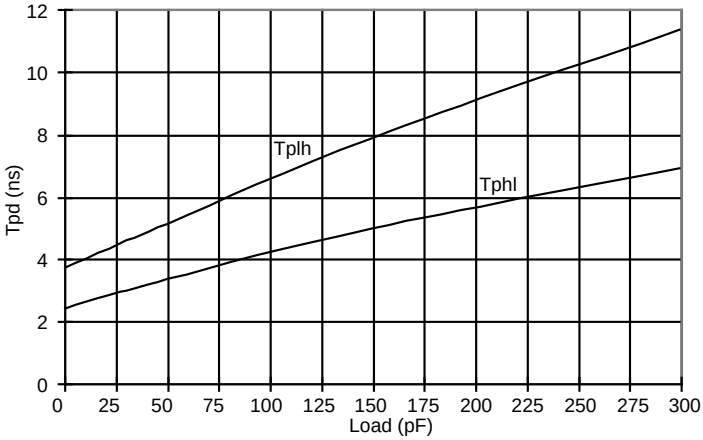

Figure 23, Delay vs. Load High Drive ('244 example)

Figure 23 shows how the effective propagation delay of an FCT244T will increase with an increase in load. The High Drive has lower output impedance than Balanced Drive and therefore will be less affected by loading.

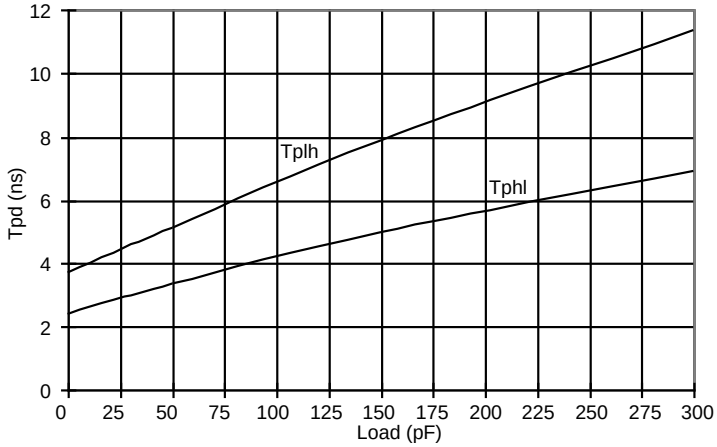

Figure 24, Delay vs. Load Balanced Drive

The Balanced Drive delay as shown in Figure 24 will be more affected by load than High Drive. The increased output impedance of Balanced Drive causes a larger RC time constant, particularly in the LOW to HIGH transition. Because of the lengthy delay under heavy loads, Balanced Drive is less suited to driving heavy loads than High Drive.

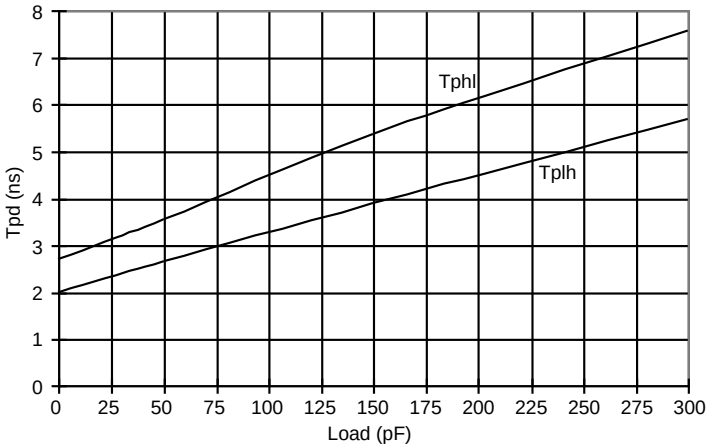

Figure 25, Delay vs. Load CMOS Output

As can be seen by Figure 25, the CMOS output components are similar to High Drive because of the similar impedance levels. The higher driving voltage of the pull up tends to increase the speed of the LOW to HIGH transition slightly, but the output voltage level has less effect on propagation delay than the increased impedance of Balanced Drive.

Number of Outputs Switching

The number of outputs switching affects the propagation delay of a component due to the switching currents in the package. Components with lower drive levels will be less affected by this phenomena than higher drive level components. Due to the high voltage swing of CMOS output components, the CMOS components will see the greatest effect. As can be seen in Figure 26, multiple outputs switching do not have a significant effect on propagation delay.

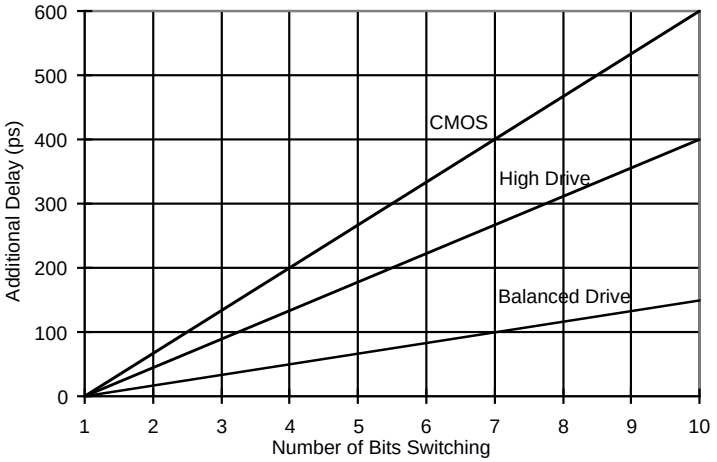

Figure 26, Delay due to Number of Bits Switching

Output Enables, Setup/Hold Times

Generally when establishing data sheet specifications for components, the primary specification of interest is the input to output propagation delay. Other specifications such as output enable/disable times, setup/hold times and clock pulse widths are considered less critical to the user. To avoid failing components in final testing due to one of these less critical parameters not meeting specification, the output enables, setup times, etc. are specified very conservatively in the data book.

Setup and Hold Times

In clocked components there is a point at which the data must be stable prior to the clock edge to guarantee that the data is clocked into the register on the clock edge. There is then an input hold time after the clock to guarantee that the clocking is complete and the changing input data will not be clocked into the register.

For most IDT octal registered and latched components, the toggle point where changing input data will be clocked into the register/latch is with the data preceding the clock by about 0.5ns (T_{SU} =0.5ns and T_H = -0.5ns). The toggle point is device specific and will be affected (minimally) by Vcc, temperature and process variations. Generally the data book specifications allow a conservative testing window around the toggle point of 3ns or more (e.g. T_{SU} = 2.0ns, T_H = 1.0ns for an FCT374DT).

Metastability

Metastability is a state that may occur in clocked registers when the input data is transitioning through the input toggle point simultaneously with the clocking of the device. Theoretically, the indeterminate state is clocked into the device. Through the device, indeterminate states are reached and an indeterminate (middle voltage) state is driven to the output. This middle voltage state is held until the device can resolve whether it is going to drive HIGH or LOW. While theoretically it is possible for any component whether it is bipolar, BiCMOS or CMOS to exhibit metastability, the characteristic is pronounced only in very slow, low gain devices.

Because of the high speed nature of FCT logic, metastability is not a problem. The high gain of the input translator will quickly resolve level issues prior to clocking, and any levels not determined at the input will be resolved in the clocking stage.

Power Dissipation

FCT-T has the lowest power dissipation of any available logic 5V logic family, making it ideal for low power and battery operated systems that require 5V components. The limiting factor in power dissipation is the component die temperature which should be limited to less than 150°C to avoid metal migration and component damage. The component die temperature is affected by the combined ambient temperature and power dissipation which can be calculated using the thermal data in section 4 of the Logic Data Book and the POWER SUPPLY CHARACTERISTICS in each data sheet (particularly note 6).

Contained within each component data sheet is an ABSOLUTE MAXIMUM RATING for power dissipation. Since the failure causing mechanism is die temperature rather than power dissipation, this specification should be regarded as a guideline only. Using heat sinks or airflow the maximum power dissipation can be increased. Under hot conditions (>70°C) the maximum power may be limited to a level lower than the data book specification. For all octal packages at 70°C in still air with no heat sink, the allowable maximum power dissipation is greater than 0.5W (the Abs Max Spec in most data sheets). Figure 27 gives approximate values for the amount of power that would need to be dissipated to bring the die to 150°C in various packages with the ambient temperature of 25°C and 70°C in still air with no heat sink.

Package	Description	θja	θjc	PT Ta = 25	PT Ta = 70
SSOP					
SO20-7	20-Pin SSOP	110	55	1.14W	0.73W
SO24-7	24-Pin SSOP	100	55	1.25W	0.80W
SO28-7	28-Pin SSOP	90	55	1.39W	0.89W
QSOP (Q)					
SO16-7	16-Pin QSOP	150	60	0.83W	0.53W
SO20-8	20-Pin QSOP	135	60	0.93W	0.59W
SO24-8	24-Pin QSOP	115	60	1.09W	0.70W
SO28-8	28-Pin QSOP	100	60	1.25W	0.80W
SOIC (SO)					
SO16-1	16-Pin SOIC	105	38	1.19W	0.76W
SO18-1	18-Pin SOIC	95	35	1.32W	0.84W
SO20-1	20-Pin SOIC	90	33	1.39W	0.89W
SO20-2	20-Pin SOIC	90	33	1.39W	0.89W
SO24-2	24-Pin SOIC	75	28	1.67W	1.07W
SO28-2	28-Pin SOIC	67	25	1.87W	1.19W
SO28-3	28-Pin SOIC	70	25	1.79W	1.14W
PDIP (P)					
P16-1	16-Pin Plastic DIP	105	55	1.19W	0.76W
P18-1	18-Pin Plastic DIP	95	55	1.32W	0.84W
P20-1	20-Pin Plastic DIP	85	55	1.47W	0.94W
P22-1	22-Pin Plastic DIP	80	55	1.56W	1.00W
P24-1	24-Pin Plastic DIP	77	55	1.62W	1.04W
P28-2	28-Pin Plastic DIP	75	55	1.67W	1.07W

Figure 27, Calculated Power for Selected Packages to Bring the Die Temperature to 150°C at 25°C and 70°C Ambient Temperatures

The power dissipation in high speed logic is broken into three separate identifiable sections. The first is component leakage (Icc) which is present whenever the component is powered. The second section is leakage due to floating inputs (ΔIcc). The third section is power dissipation due to device switching (I_{CCD}). In addition to these three, there is also power dissipation due to output loading which must be calculated by the system designer. (See Application Note #AN-154.)

Leakage Currents (Icc)

IDT Octal Logic has the lowest leakage currents in the industry with typical leakage levels lower than 1μA. This makes these components ideal for battery operation and other very low power applications. When comparing with FAST or other Bipolar families with very heavy leakage levels, using an FCT family may allow the reduction of system power requirements.

Dynamic Switching Current (I_{CCD})

The largest component of power dissipation at high frequencies is the Dynamic Switching current which is listed in the data sheet as Iccd. Iccd is the leakage through the internal component parasitics during switching. IDT's FCT logic has the lowest dynamic switching currents in the industry. These switching currents are lower than any bipolar, BiCMOS, or other CMOS family. One of the easiest ways to measure switching current is by measuring the Ic with the switching output pin cut off. Since Iccd is the internal switching current and is measured in an unloaded state, the three FCT families (High Drive, Balanced Drive and CMOS) all have a similar Iccd of approximately 42µA/MHz for each bit switching. Iccd is not a measure of the switching current caused by the load.

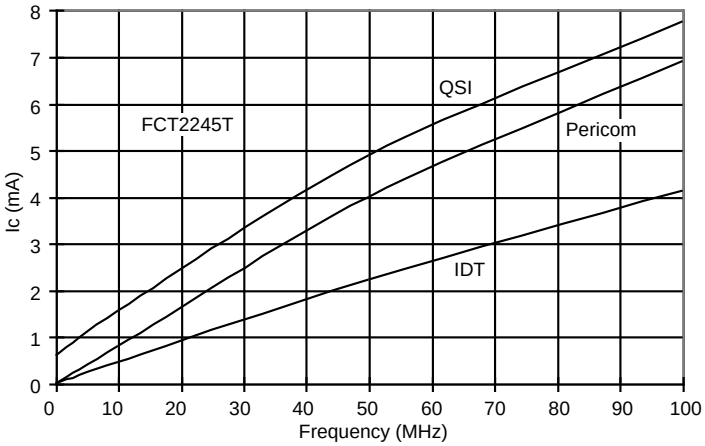

Figure 28, Ic vs. Frequency

Figure 28 shows the dynamic switching current for FCT octal devices from three different vendors with one bit switching with the output cut. All other inputs are tied to Vcc or GND. The data is lab test data with Vcc = 5.5V, Ta = 25C.

Input Leakage (ΔIcc)

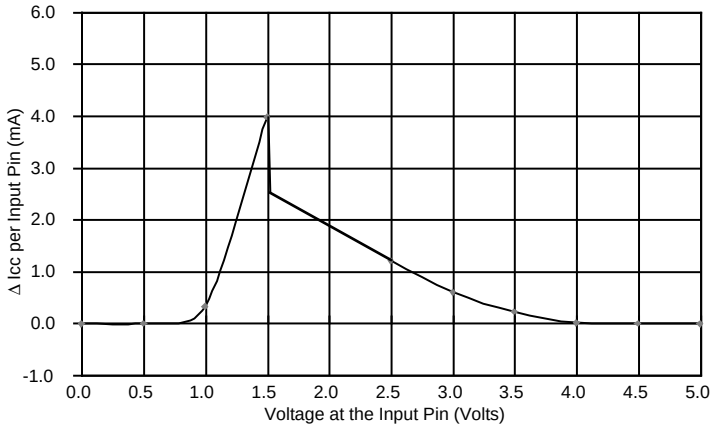

Figure 29, ΔIcc vs. Input Voltage

Looking at Figure 1, the input structure consists of a P-Channel and an N-Channel FET stacked on top of each other. When device inputs are held at levels other than Vcc or GND, both FETs will partially turn on allowing a leakage directly from Vcc to GND. The amount of leakage for a typical device input is shown in Figure 29. In order to maintain low power dissipation, device inputs should always be held either HIGH or LOW at levels away from the areas of high leakage as shown in Figure 29.

Load Currents

In addition to the device leakages and currents, there is power dissipation caused by driving the load. The current supplied to the load can be calculated by the equation:

$I_{LOAD} = fCV$
C = Load Capacitance
f = Switching Frequency
V = Output Voltage Swing

Figure 30, Load Current Equation

Figure 30 shows the current supplied to a capacitive load under switching conditions. Power can then be calculated by multiplying the current times the voltage ($P = fCV^2$). Since voltage is the square term in the power equation, power dissipation is very dependent upon switching voltage. Because of this, the Balanced Drive and High Drive components will give lower power dissipation due to the load with their TTL level outputs than the CMOS Output will give with an identical load.

Conclusions

FCT Logic provides both performance and flexibility which is unequaled in the industry today. In addition to the high performance and low power dissipation which is common to all FCT families, there is a variety of choices, allowing the designer to adapt the component to his application. Through component selection FCT logic is capable of driving everything from a heavy backplane to a very lightly loaded quiet point to point signal. Speed grade selections allow a designer a cost/performance tradeoff, all within the same logic family. These benefits combine to make FCT the most widely used, universal, high performance family.