SYNCHRONOUS DUAL-PORT STATIC RAMS FOR DSP AND COMMUNICATION APPLICATIONS

APPLICATION NOTE AN-144

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Abstract

Dual-ported memory is a specialty static RAM which has been available in numerous configurations for many years. The dual-ported SRAMs (DPRAMs) have increased in size and speed, and coupled with their simultaneous access, they provide increased bandwidth which far exceeds other available standard SRAM (Static Random Access Memory) capabilities. Recent enhancements, however, allow for even higher bandwidth to be obtained.

Data transfers are moving towards being more synchronous and may be either random, sequential, pipelined and/or non-pipelined applications. Integrated Device Technology recognizes this, and has responded by introducing a range of new components to meet the needs of these emerging markets. If dual-ported technology is the answer, then synchronous dual-ported SRAM will carry today's designs even further.

Introduction

Synchronous DPRAMs

Synchronous dual-ported random access memories (SDPRAMs) are available in several varieties. All of them provide simultaneous access capabilities and have registered inputs. Some of them also have registered outputs, flags, and programmability.

The Sequential Access Random Access Memory

The first of the synchronous components to be presented is the SARAM™. The SARAM (Sequential Access Random Access Memory) is a specialty dual-ported SRAM which allows bi-directional access from both a synchronous port and an asynchronous port. (Figure 1)

The SARAM allows the programming of the Sequential port (the synchronous port) for use as a FIFO-like device, while allowing for the standard random accesses through the asynchronous port.

Programming of the SARAM is performed via the random port. Although the random port is a standard dual-port interface (which includes the address bus, 16 bit byte selectable data bus, $\overline{CE}$, $\overline{OE}$, and R/$\overline{W}$), it has a $\overline{CMD}$ pin which is unique. When the SRAM array is disabled, taking $\overline{CMD}$ = V_{IL} allows for the sequential port's control registers to be accessed.

The registers are accessible to allow for two buffers to be designated for separate access by the sequential port. These buffers may be isolated or overlapped, and may engulf a portion or the whole array. A beginning and an end address are stored for each buffer.

Another register allows for the event of reaching the end of the buffer to program the next state that will occur. The options include wrapping around the buffer back to the beginning, jumping to the next buffer's beginning address, stopping, outputting a flag, and continuing to sequence

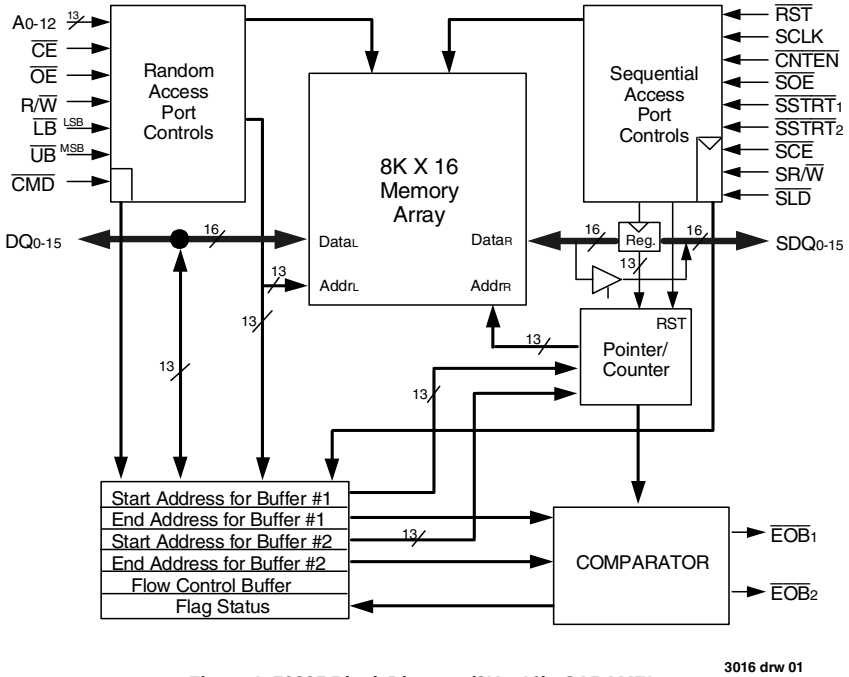

Figure 1. 70825 Block Diagram (8K x 16) - SARAM™

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after the end address has been reached.

The last register allows for the flag to be read from internal registers and for the registers to be cleared.

The sequential port data bus is also 16-bits wide. The main difference is that the sequential port is synchronous, and is similar in some of its functions to FIFOs - sequential from the beginning address to the end of a buffer with flags. All of the control signals of the sequential port are synchronous except for the output enable.

There are two $\overline{STRT}$ pins which when asserted cause the address pointer to jump to the start (beginning) address of the associated buffer - similar to the retransmit of a FIFO. End of buffer flags are available which can be utilized for full, empty, half-full, and partially-empty indicators per their programming as to when they will be asserted.

There are the standard R/$\overline{W}$ and $\overline{CE}$ inputs, except they are synchronous (SR/$\overline{W}$ & $\overline{SCE}$). A clock pin (SCLK) is included along with a $\overline{RST}$ pin which sets the buffers to a default value and disables the sequential port.

Finally, there is a sequential load pin ($\overline{SLD}$). The $\overline{SLD}$ allows for the data bus to double as an address bus for the synchronous address load (or DMA) function.

Current Synchronous DPRAMs

The synchronous parts to be discussed are the IDT709149 (Figure 2) and the IDT70914 (Figure 3).

The only difference between the 70914 and the 709149 is the output pipeline register included in the 709149. The left port of the 709149 is always pipelined, where the right port is selectable for either flow-through or pipelined. The 709149 pipelined port is always available at least 1 speed grade faster than the 70914. Like the 70914, the 709149 has a common $\overline{OE}$ and R/$\overline{W}$ for all 9 bits.

The synchronous pipelining output option is generally used for bursting packetized data, where the synchronous fow-through output option is

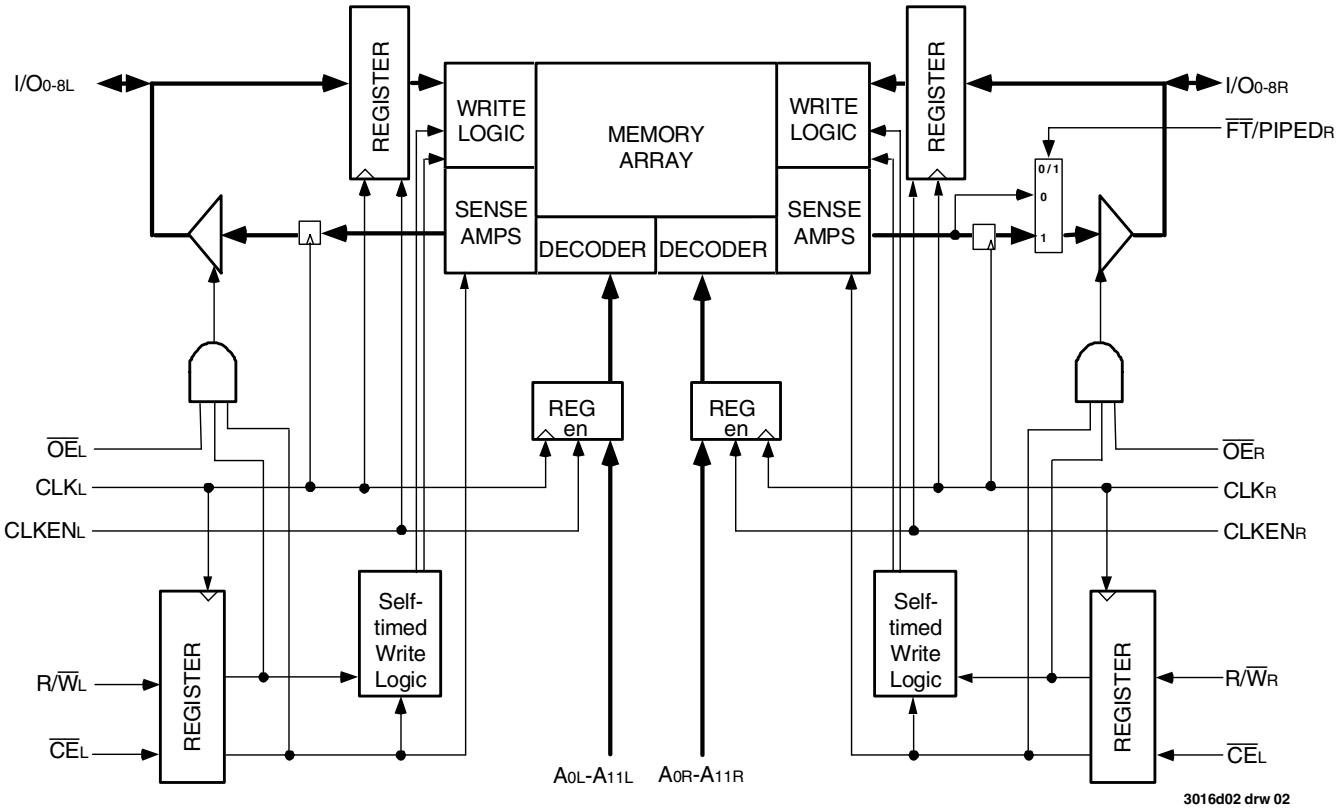


Figure 2. 709149 Block Diagram (4K x 9), Sync Pipeline Output Option

generally associated with synchronous random access. The 70914 is a flow-through output 4Kx9 Dual-Port, and the 709149 is a pipelined output 4Kx9 Dual-Port.

Since the pipelined parts are just a flow-through component with the data output additionally being registered prior to continuing out through the existing output buffer, there is an additional clock cycle required for the data to be read out. The extra cycle introduced to the path from the address input to the valid data output for the pipelined components is called a latency.

The additional latency benefits the system's design by giving a faster t_{CD} than it's flow-through counter part. The faster t_{CD} available from the pipelining mode (and unfortunately the added latency) allows for the component receiving the data to have additional input setup time. This additional time allow the system to take advantage of more timing margin to get faster cycle times and higher bandwidth.

In order to take advantage of the pipeline output option, the system components supplying the starting address to the dual-port must know the address two cycles prior to the expected data output usage - where it is just one for the more common flow-through components.

For the flow-through mode, there is no added latency. t_{CD} is more like the standard asynchronous t_{AA} specification, versus just a little more than a standard t_{OE} as is the pipelined components. The benefit of using the flow-though components is to give the system the benefits of synchronous access, but allowing for the fact that the system components supplying the addresses receiving the data output from the dual-port can not handle the latency.

Next Generation SDPRAMs

The following information highlights a few of the next generation synchronous dual-ports. They are synchronous and sequential on both ports, and are the largest dual-ports available in the industry. The basic linear sequencing and control are as defined by JEDEC burst SRAM pinout definitions and industry standards.

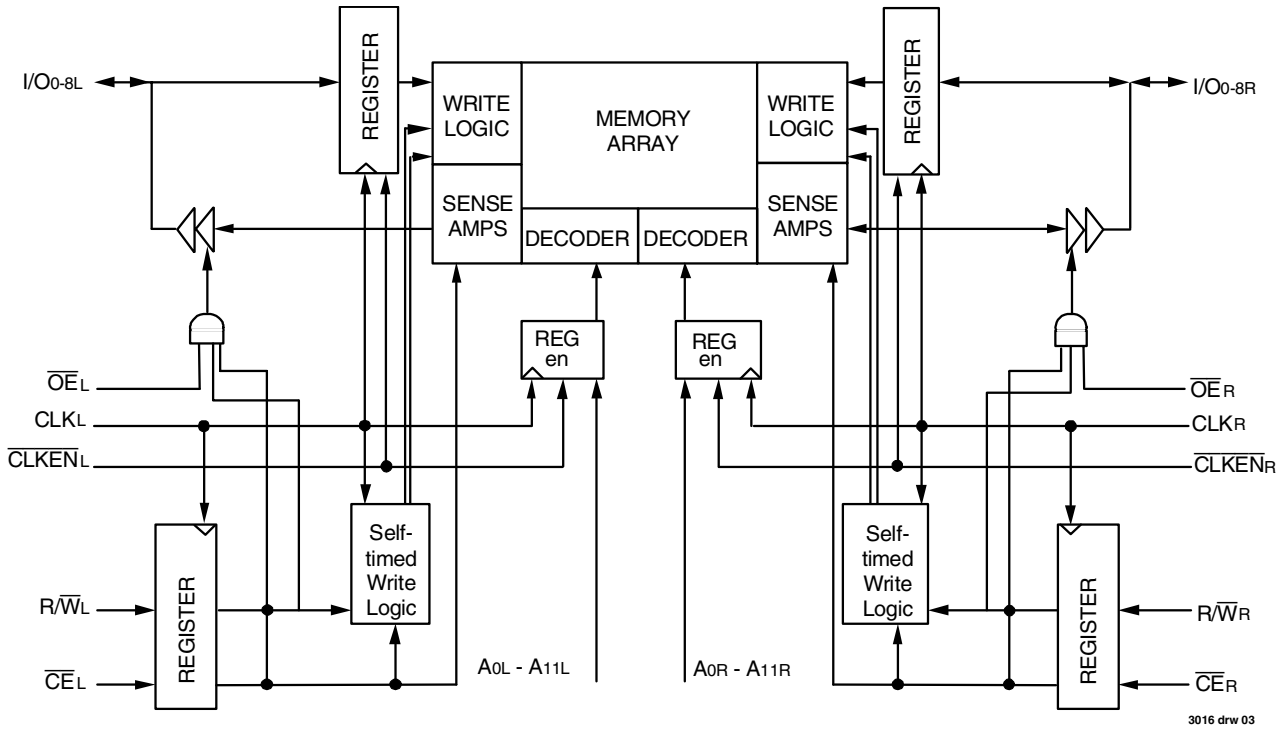


Figure 3. 70914 Block Diagram (4K x 9), Sync Flow-through Output Option

IDT is making the new Synchronous Dual-Port standard with the IDT70V3379, IDT70V3389, 70V3569, 70V3579, IDT70(V)9089 (Figure 4), IDT70(V)9079, 70(V)9089, IDT70(V)9269 and IDT70(V)9279. These devices are pipelined and flow-through dual-ports.

The difference between the existing IDT70914 (Flow-Through) and future IDT709149 (Pipelined) synchronous dual-ports and the new synchronous components is the sequential capability. Instead of the Address having to be supplied on every cycle, there is a burst capability available in the IDT70V3379, IDT70V3389, IDT70V3569, IDT70V3579, IDT70(V)9089, 70(V)9269 and IDT70(V)9279.

A non-burst occurs by loading a new address on every cycle, done by asserting the $\overline{ADS}$ LOW on every cycle. The burst capability is utilized

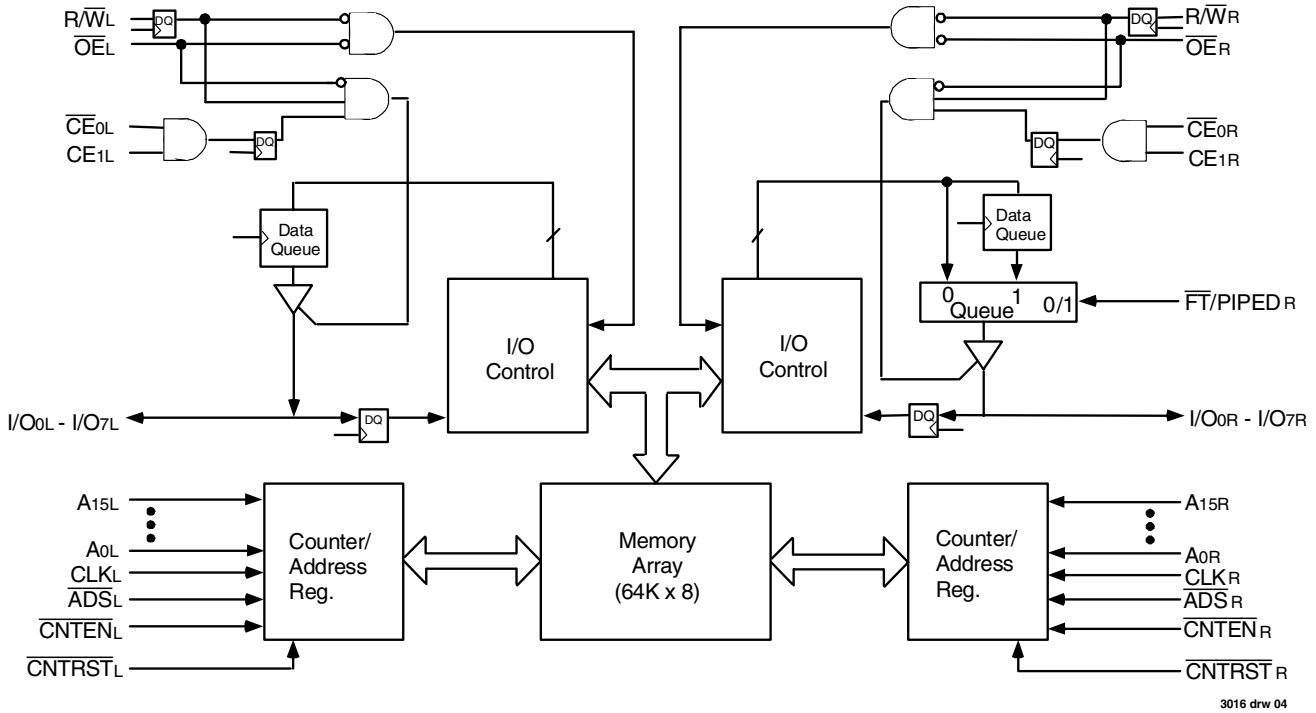


Figure 4. 709089 Block Diagram (64K x 8), Sync Pipelined Option

by loading the data packet's beginning address when the $\overline{ADS}$ is LOW, followed by $\overline{ADS}$ HIGH and $\overline{CNTEN}$ LOW for the subsequent cycles. The $\overline{CNTEN}$ LOW enables the sequencing, but is ignored if a new address load is initialized ($\overline{ADS}$ being LOW).

NOTE:

a 'LOW' is a V_{IL} as specified in the Specialty Memory Data sheet, a 'HIGH' is the equivalent to a V_{IH} specification.

A little-known additional benifit of our new pipelined parts over our previous non-sequential components is the capability introduce a new address on each cycle by keeping $\overline{ADS}$ LOW. Although the latency is still added for each address to data output, the addresses being input can be random and need not be sequenced with $\overline{CNTEN}$ LOW - instead $\overline{CNTEN}$ is kept HIGH to disable the address advancement.

$\overline{CNTRST}$ resets the address pointer to zero, but does not disable the port from its access on that cycle.

The 70(V)9089 and 70(V)9279 components have separate address and data busses, similar to the 70914(9) parts but unlike the SARAM's sequential port. Dual chip enables are also provided for the easy depth expansion of the 70(V)9089 and 70(V)9279 components.

The two chip enables have different polarities ($\overline{CE}_0$ & CE_1). This option is offered on the new synchronous components, and the new asynchronous components - the IDT7008 (64K x 8) and the IDT7027 (32K x 16). This dual chip enable scheme allows for easy depth expansion with no external logic, and eliminating the requirement for a faster dual-port to allow for the delay of the additional external logic required to do the address decode for the single chip enable.

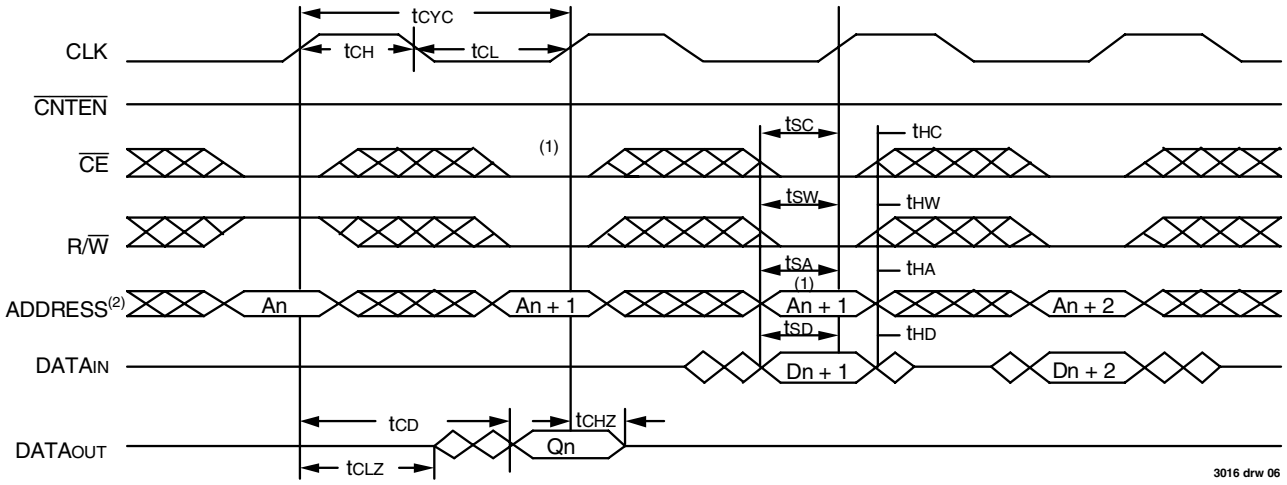
Both flow-through and pipelined synchronous dual-port components are available on each device. The '9' or '3' designator in the middle of the standard part number designates the synchronous components. All new components follow this rule where older components may not (i.e., a '9' at the tail end may also represent x9 components).

Flow-through outputs are non-pipelined (no output register), where pipelined has a register in the output data path. The output data path affects only the read path, not the write path. Therefore the write path is identical for the synchronous components, whether they are flow-through or pipelined.

The address to data flow-through relationship lends itself to random access algorithms, where pipelining lends itself to packetizing information for burst applications. Although pipelined data often requires a latency, bursting data recovers the cycle time and allows for address pipelining to be done. Once a pipeline is initiated, there are no more latencies until the pipe is flushed.

The synchronous flow-through parts have a clock-to-data valid (t_{CD}) of similar access time to the standard asynchronous component's Address Access (t_{AA}, address to data Valid). The cycle time (t_{CYC}) may be as low as the t_{CD}, but is specified as t_{CD}+5ns to allow for the user's real system usage to satisfy a 5ns setup time (t_{SU}) to the input of the device receiving the data.

Figure 6 shows a normal clock cycle, where the clock is generated by an oscillator chip. There is a standard bus turn-around from a read cycle



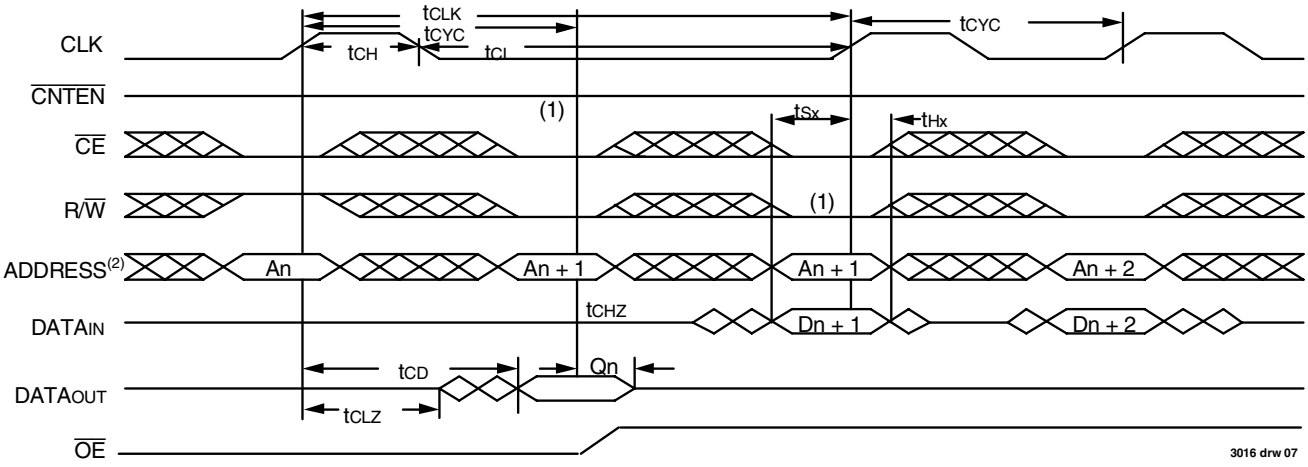
1) The first R/$\overline{W}$=LOW while $\overline{CE}$=LOW and $\overline{CLK}$ is going HIGH will write ones into [An+1] while Qn is output from the previous [An] Read. The following R/$\overline{W}$=L writes (Dn+1) into [An+1].
2) Address is Clocked in when $\overline{ADS}$=VIL. Address is Incremented by $\overline{CNTEN}$=VIL.

Figure 6. 70908 Synchronous Operation - Read-to-Write Fast tCYC Waveform

to a write cycle for both fast and slow cycle times. This is demonstrated in Figure 7 for the 709089 in Flow-through mode, but is identical for the 70914 and the 709279 in Flow-through mode..

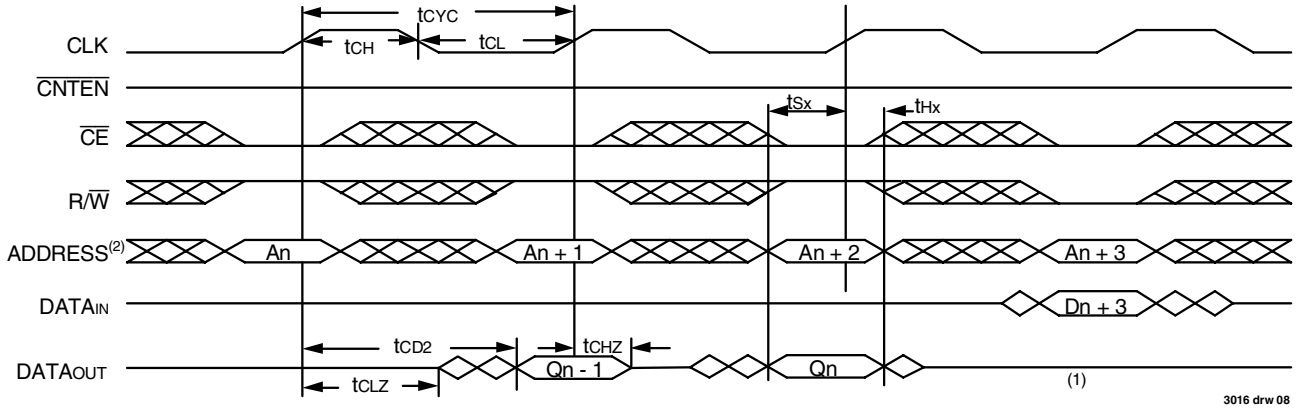
Pipelined components have one cycle of output latency added from the registered input address. Whether the address is clocked in on every cycle or once in a while for a burst condition, the latency occurs. This means that the pipelined usage may be used for bursting or random access, but in either case a latency is introduced when an address is loaded. (Figure 8).

The tCD of a pipelined component is similar to the output enable time (tOE) plus a few nanoseconds (typ. 3ns extra).



1) Qn is read out at the tCD interval from the previous [An], then disabled to allow the subsequent Write. The R/$\overline{W}$=VIL writes (Dn+1) into [An+1], Qn is not written back into [An+1] in this case.
2) Address is Clocked In when $\overline{ADS}$ = VIL, and Incrimented when $\overline{CNTEN}$ = VIL.

Figure 7. 70908 Synchronous Operation - Read-to-Write Slow tCYC Waveform



1) The first R/$\overline{W}$ = VIL while $\overline{CE}$ = VIL and CLK is going HIGH will write Qn+1 from the previous Piped [An+1] Read into [An+3] if $\overline{OE}$ = VIL and there was no Data Contention.
2) Address is Clocked in when $\overline{ADS}$ = VIL and Incrimented when $\overline{CNTEN}$=VIL.

Figure 8. 709089 Sync-Pipelined Operation - Read-to-Write Waveform

Synchronous Dual-Port Memory Summary and Usage

In a summary for the synchronous dual-ported SRAMs there are synchronous, sequential, pipelined, flow-through, and separate and common address and data bus component variations available in varying densities.

The benefits of the synchronous memories involves the tCD specification (which is referenced from the clock's rising edge to data output valid) and the setup and hold time of the synchronous input signals to the clock's rising edge. The creation of the control signals and the sampling of the synchronous data by another synchronized component is easier than the creation of asynchronous control signals and the sampling of the data, especially as the system requires more bandwidth and therefore frequencies increase. System frequency increases are directly related to the memory cycle time requirements, and the memory cycle time decreasing as frequency increases requires the system to generate smaller and smaller pulses to control an asynchronous memory.

By allowing the memory controller and sub-system to go synchronous, the controller effectively has more time to gen-erate the synchronous memory's input signals and does not have to hold them very long. This makes the memory controller's job much easier, allowing the controller to go off and do other critical tasks or allowing the designer to implement the controller in a cheaper more readily available technology.

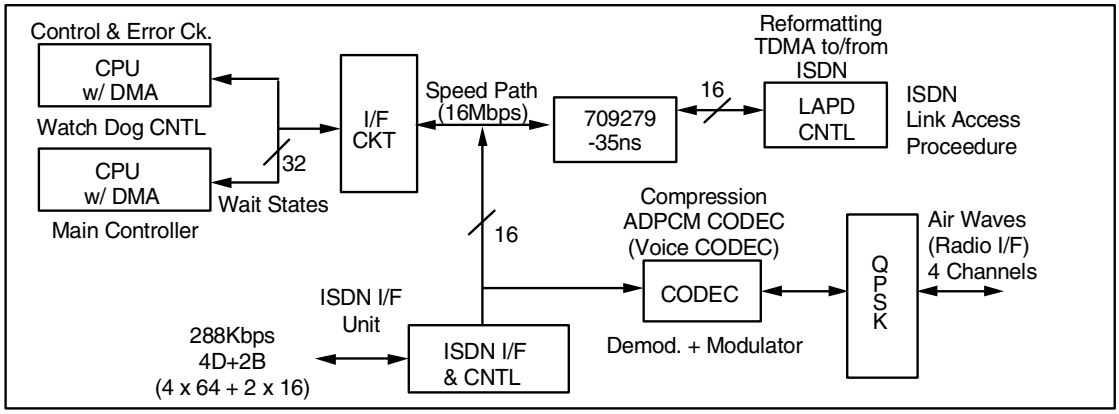
Likewise, being 'Burst Ready' (Sequential) allows for the address bus to go off and do some other task when it is not generating an address for the synchronous dual-port's input. The address is only required at the beginning of a packet burst and therefore only recognized when $\overline{ADS}$ is LOW. The other cycles during the burst can either disable the address generation to save power and reduce noise, or it could be doing some The

	70914 709149	70824 70825	70(V)9089 70(V)9279	70V3579 70V3389
Address/ Data	Separate Busses	Common Busses	Separate Busses	Separate Busses
Pipelined/ Flow-through Output		Flow-through	Pipelined/ Flow-through	Flow-through
Latency	None/One	None	One with Pipe None (No Pipe)	One
Access	Random	Sequential/ DMA	Sequential/ Random	Sequential/ Random
Self-Timed	No	No	Yes	Yes
tCD	15/12	15	9	5

3016 tbl 01

Table 1. Sync. Dual-Port Summary Table

- Voice & Data thru the 709279 (Sync.)
- LAPD Modifies D and B data & Stores in 709279 Buffer (Async.)



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4 Channels per Base Station: 2 x [2B (Data) + 1 D (Control) = 144 Kbps] = 288Kbps
Each Phone is 32Kbps Compressed Data: 4 x 32 Kbps x 2 (Compression) = 128Kbps x 2 (Bidirectional) = 256Kbps + Control

Sync. Dual Port Performance May be used for Compression & Reformatting of Bidirectional Data, plus simplifies Design & Reduces Board Space.

Figure 9. Portable Phone Base Station - Using the 709279 DPRAM

other task with other chips in the system.

DSPs are available in both asynchronous and synchronous versions. Control ASICs are currently being developed as synchronous devices. Therefore the DSP component chosen and the controller methodology will dictate the type of memory component to be chosen. In the future, components will be synchronous to ease the design limitations of higher bandwidth system requirements.

For the above base station design, the existing shared bus may easily be converted to a synchronous device interface. The shared bus is a HIGH bandwidth bus that transfers packets of data at each burst, with the transfers being comprised of single or multiple packets. The reformatting controller requires asynchronous transfers.

Although the reformatting transfers are also synchronous for the controller design, the existing design of the controller generates signals for asynchronous devices and therefore lends itself to remain asynchronous. This design is ideal for using the SARAM, where one port is asynchronous and the other port is sequential.

When both ports are burst ready, the pipelined parts are the best choice. In the next case, both ports are easily changed to synchronous device interfaces but only the external interface is pipelined ready.

Therefore the external bus is pipelined and the internal bus utilizes the 709279 $\overline{FT}$/PIPED$_R$ control pin to be non-pipelined (flow-through). This provides a single component solution and an easier design methodology.

For the SDPRAM, the t_{CD} specification for the DSPs is similar to the t_{AA} specification.

Synchronous devices merely require an input setup and hold time with

- 8 Channel Card
  - 1 SDPRAM per CHNL
- DSP MUXed to SDPRAMs
  - Random Flow-Though Access
  - 1 Wait State Access
- Data is Access Packetized
  - Sequential Pipelined Access
  - 0 Wait State Access

Utilizes Sync. Dual-Port Simultaneous Access: there is a Significant Board Space Savings & Decreased Design Time.

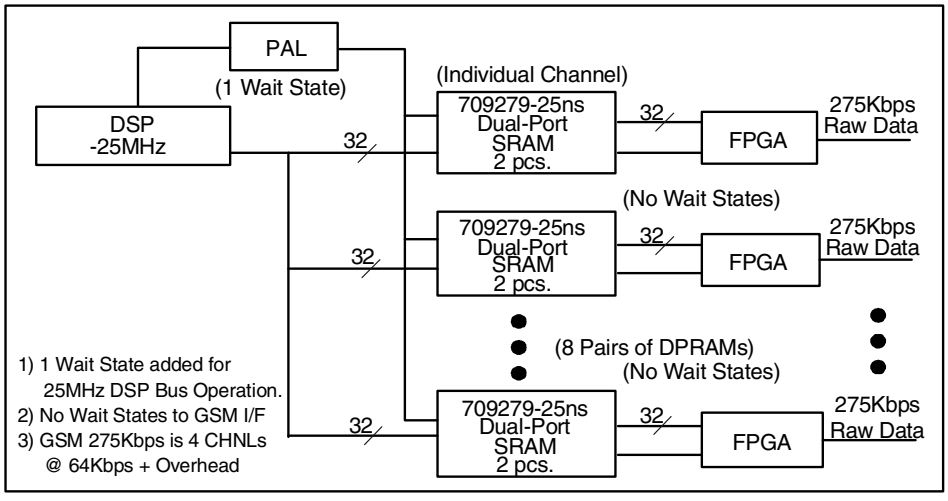

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Figure 10. Portable Phone Base Station - Using the 709279 DPRAM

respect to the synchronized Clock which is their reference. The cycle time, or clock period, remains the same for the system whether DPRAMs or SDPRAMs are used. Therefore the t_{CD} required is still approximately equivalent to t_{AA}.

SDPRAM DSP Timing

- DSP timing is typically for t_{AA}, vs t_{CD}
  - SDPRAMs are referenced to the clock
    - t_{SU} is now the parameter required to meet for DSP
      - $t_{CD} = 2H - t_{SU} - t_{DER}$, where $2H = t_{CYC}$ of the SDPRAM
      - t_{CD} is the SDPRAM timing parameter available
        - Both flow-through & pipelined t_{CD} components are available
  - DSP must meet the SDPRAM specs
    - Address t_{SA} and t_{HA} and Data t_{SD} and t_{HD}
      - Much easier to meet t_{SD} and t_{HD}

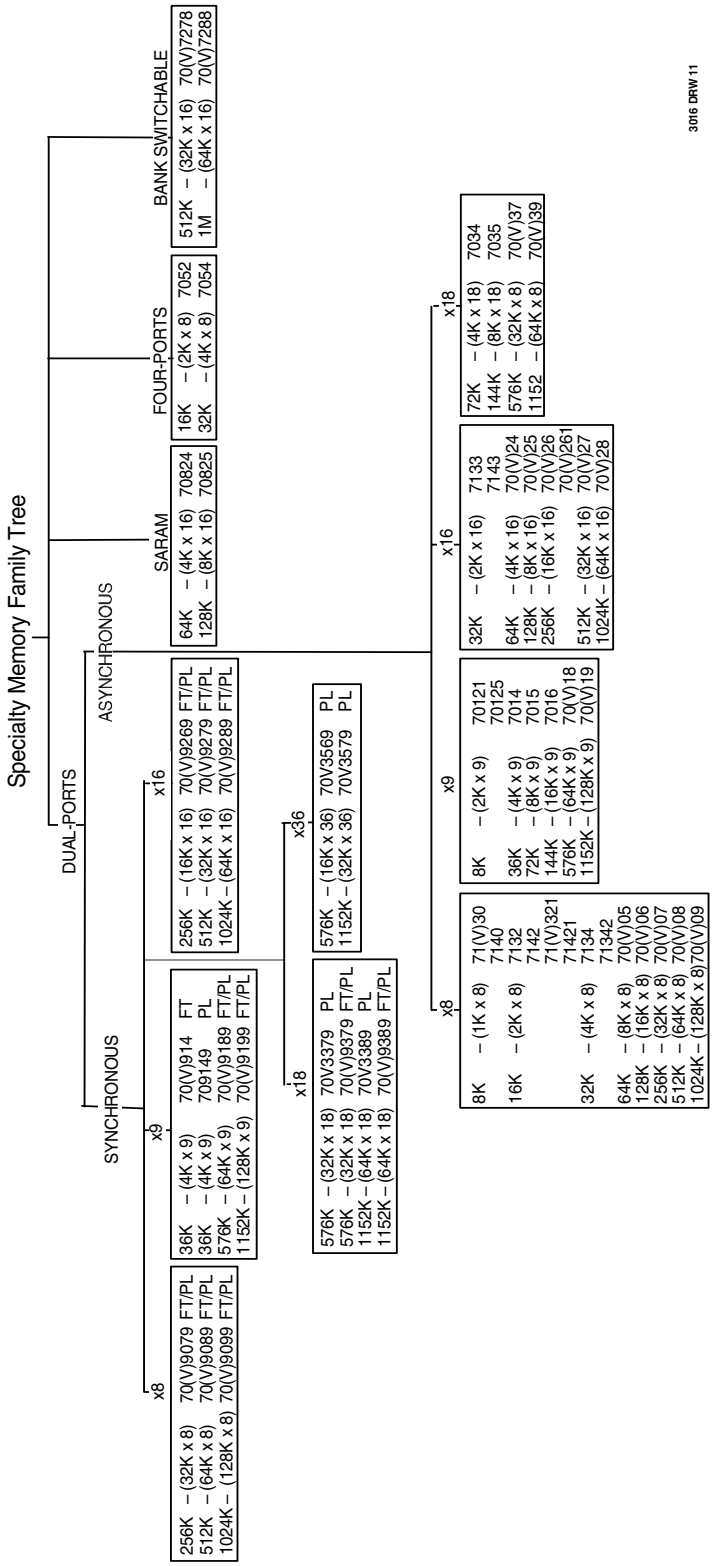
The primary reason for choosing synchronous over asynchronous devices is that synchronous systems provide convenient means to meet controller timing requirements. The required setup and hold times are easier to generate for higher frequency systems than the asynchronous control signals. As the cycle time shortens, asynchronous control signals are more difficult to generate and this becomes compounded by bus limitations.

Conclusion

By using our latest technology, IDT is able to guarantee high bandwidth solutions at lower system cost than from any other semiconductor manufacturer. IDT's products satisfy the strictest industry requirements for quality and reliability. Dual-Ports provide bandwidths and system performance advantages including bandwidth, design ease, board space, cost savings, etc. that can not be achieved with standard SRAMs. The IDT Specialty Memory Division currently offers the most comprehensive Multi-Port product line in the industry.

The following IDT Specialty Memory Family Tree not only indicates our current products (includes our 5V, 3V, Async., and Sync. products), but indicates IDT's commitment to keeping our specialty memory leadership with innovative new designs and higher levels of integration. The new products in development are highlighted in gray.

The desribed synchronous components are listed in the IDT Family Tree within their own section, to highlight IDT's commitment to evolving markets. IDT's technology and design philosophies allow high-bandwidth requirements to be met with cost-effective solutions today.



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